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Review

Single-Inductor Multi-Output DC-DC Switching Converters Using Exclusive Control Method

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Received: 24 November 2024; **Revised:** 17 January 2025; **Accepted:** 25 January 2025; **Published:** 5 March 2025

Abstract: This review paper presents Single-Inductor Dual-Output (SIDO) and Single-Inductor Multi-Output (SIMO) DC-DC converters with our proposed exclusive control method. First, we provide an overview of three fundamental types of switching converters: the buck converter, the boost converter, and the buck-boost converter, all using Pulse Width Modulation (PWM) signals for their control. Next, we introduce SIDO converters with the exclusive control method, including the PWM control, the ripple control, the hysteretic control, and the soft-switching (with zero-voltage switching). In addition, we introduce its extension to a configuration of the dual-output Single Ended Inductor Converter (SEPIC) with the buck-boost converter, the high boost converter and the multiplied boost converter. Finally, we show exploration of four-output converters using our proposed voltage comparative circuit. The exclusive control method requires a few additional components but does not rely on current sensors. Also, it is not influenced by the output voltage or current value. Furthermore, we look ahead to future research directions for improving the subject.

Keywords: Switching DC-DC Converter; Single-Inductor Dual-Output (SIDO); Single-Inductor Multi-Output (SIMO); Exclusive Control; Soft-Switching Converter; Single Ended Primary Inductor Converter (SEPIC)

1. Introduction

Today, most electronic devices, ranging from smartphones to industrial machinery, are dominated by digital technologies. DC-DC switching converters are essential components in nearly all these electronic devices due to their stable and reliable operations. Lots of applications necessitate several supply voltages for large digital and memory circuits, small-yet-crucial analog circuits, including sensors and other devices. In a conventional system, each voltage output in the DC-DC converter requires a separate inductor, resulting in the need for many power inductors throughout. However, it is desirable to minimize their number for the system cost and volume reduction. Previously, achieving dual supply voltage outputs required the use of two separate DC-DC switching converters, each necessitating a power inductor and a capacitor. However, recent advancements in manufacturing technology have allowed capacitors to be smaller, even as operational clock frequencies continue to rise (from approximately 200 kHz to over 5 MHz). Despite these improvements, reducing the size of the power inductors remains challenging due to the need to handle large currents. Therefore, efforts to reduce the size and cost of switching converters focus on minimizing the number of the power inductors.

Recently, there have been many reports on SIDO DC-DC switching converters, which are particularly used for small power circuits. The control methods of these previous converters can be classified in two categories: (i) One

is to employ serial pulse-width control to divide a single pulse into dual widths for each converter within a single cyclical switching period. In this serial control system, achieving precise stabilization of two output voltages is challenging due to the presence of two on-time and a single off-time control within a single clock period. (ii) The other is to appropriately switch the supply time of the current for each sub-converter within one clock cycle.

To achieve precise control of dual output voltages in the SIDO converter with large current outputs, we have developed a multi-output control system called the 'exclusive control method' as the third method. This method involves selecting one of sub-converters and controlling the serial current switch at each sub-converter input during each cyclic period. By comparing the voltage error outputs, only one sub-converter is exclusively chosen to be controlled in the next period. This selective operation is performed cyclically to stabilize each sub-converter output voltage. Its ultimate goal is to achieve simplicity (eliminating the need for a current sensor), fast response, minimal ripple, high efficiency, and applicability to various types of switching converters.

In this paper, we first explain fundamental DC-DC switching converters: the buck converter, the boost converter, and the buck-boost converter with the PWM control. The buck converter is used for down-conversion of the input voltage. The boost converter is widely employed in mobile equipment to increase the battery voltage. Finally, the buck-boost converter adjusts the input voltage either up or down, making it suitable for systems with variable input voltage. To comprehend our exclusive control for various SIDO converters, it is essential to understand the operation of these switching converters.

Next, we will discuss SIDO converters with the exclusive control method. These converters utilize various control techniques, including the PWM control, the ripple control, the hysteretic control, and the soft-switching (or zero-voltage switching: ZVS). The SIDO converter employing the 'exclusive control method' selects only one sub-converter from all available sub-converters during each clock pulse period. The chosen converter receives an input energy through the main switch and the inductor. For the sub-converter selection, each amplifier evaluates its voltages relative to the output and reference voltages in each sub-converter, and all the amplified error voltages are compared. The SIDO converter only requires a comparator and a selector, without the need for current sensors. Here, we provide an overview of various SIDO converters, including those utilizing the PWM control, the ripple control, the hysteretic control, or the soft-switching. We also report on their configuration, operation, simulation results, and experimental findings.

Furthermore, we present a preview of SIMO DC-DC switching converters featuring four output voltages. When developing the SIDO configuration, a challenge arises due to the increasing number of comparators needed to compare all output voltages with each other. This growth is proportional to the number of converters. To address this issue, we propose using a diode OR circuit and a single comparator. Finally, we introduce the SIDO converter based on the SEPIC, which includes both the high boost SEPIC converter and the multiplied boost SEPIC converter.

This paper is structured as follows: Section 2 briefly reviews control methods for SIDO and SIMO converters. Section 3 presents an overview of fundamental DC-DC switching converters; the buck converter, the boost converter, and the buck-boost converter, using their configurations, operations, simulation results, and experimental waveforms. Section 4 previews the SIDO buck-buck and boost-boost converters with the exclusive control method. These include simulation results and experimental waveforms. Section 5 introduces two hysteretic converters with the ripple-based control and with the triangular signal. Then their SIDO buck-buck converters are explained using their operations, simulation results and experimental waveforms. Section 6 discusses basic ZVS buck converters and SIDO ZVS buck-buck converters using the PWM control with their operations, simulation and experimental results. Also, Section 7 presents two basic soft-switching buck converters with half-wave voltage and with full-wave voltage, as well as their SIDO buck-buck converters with their simulation results. Section 8 introduces SEPICs with buck-boost, high boost and multiplied boost methods, and the dual-output high boost SEPIC with mode-change control. Section 9 introduces SIMO buck converter and multi-output multiplied boost SEPIC with their operations and simulation results. Especially, our voltage comparative circuit for multi-output systems is described. Finally, Section 10 concludes the paper and anticipates discussions on future research directions; Electro-Magnetic Interference (EMI) noise and output ripple noises issues.

Throughout this paper, the simulation and experiment conditions are based on the following consideration:

(i) The DC-DC converter targeted in this paper is intended for DC power supplies installed in portable electronic devices such as cellular phones, where compactness and light weight are essential. However, it can also be applied to DC power supplies in other electronic devices that require compact and lightweight components. The current power

consumption in cellular phones is about 1W at most, and the power consumption for each function is approximately 1,100mW for the phone function with the backlight at 100% [1].

(ii) In typical portable electronic devices, the output voltage of a "DC-DC buck converter" is divided into multiple outputs, approximately Vo = 5V, 3.3V, 1.8V, and 1.0V, with each output current being up to about 2A. On the other hand, the drive method for an LCD panel, which varies depending on the type of LCD, usually involves a control voltage of 5V to 12V, for which a "DC-DC boost converter" is used in portable devices. The control method is a phase change in the liquid crystal due to the voltage, and its current consumption is small. Of course, there are also devices with Vo = 3.3V and I = 10A.

(iii) Previously, a clock frequency of 500 kHz was standard, but currently it ranges from 1 MHz to 5 MHz. The inductors and capacitors in the simulation circuit are based on an actual switching converter. In practical power supplies, the output capacitor is usually divided into four sections (4 × Co), and the internal resistance of the capacitor is reduced to a quarter (r/4) to lower the output voltage ripple.

2. Related Works

In conventional SIMO DC-DC converters, including SIDO ones, multiple output voltages are typically regulated by switching the output current from a single power stage to each voltage output stage. In this case, the control is achieved by switching the control target using negative feedback signals from each output voltage, the control stage, and multiple switches. Two representative control methods are implemented:

1. "Sequential Time-Multiplexing Control Per Cycle for Each Sub-converter", which sequentially switches the control target per cycle of the control clock.

2. "Sequential Switching Control Within a Cycle for Each Sub-converter", which appropriately switches the supply time of the current within one clock cycle.

On the other hand, this paper introduces SIMO converters with our proposed exclusive control method, which is an improvement over these traditional control methods. This method controls the sub-converters by switching them each cycle, but the control order is entirely indefinite, prioritizing the sub-converter having the largest amplification error voltage. Notably, the SIMO converter introduced in this paper does not require current sensors.

2.1. Sequential Time-Multiplexing Control per Cycle for Each Sub-Converter

This class of SIMO converters determines the feedback PWM pulse width for multiple output voltages in a fixed order every clock cycle to control the power stage. This control method can handle relatively large power output. One advantage is that the control circuit has a simple configuration; it typically generates PWM pulses from each output voltage, switching and selecting them sequentially to supply to the power stage. However, its downside is that when there is a significant voltage fluctuation due to load variation on one output, the fixed control order can lead to slow voltage recovery and relatively large output voltage ripple [2–6].

2.2. Sequential Switching Control within a Cycle for Each Sub-Converter

For the multiple output voltages of the SIMO converter, the current is supplied to the output of each sub-converter sequentially within a single clock cycle. This method is typically employed in converters with relatively low output power. One advantage is that fine voltage control is possible since the current is supplied to each sub-converter output within every clock cycle. However, the method for determining the PWM pulse width corresponding to the inductor ON time is somewhat complex, and the process of appropriately selecting the current distribution time for each output is further complicated. Notice that many SIMO converters operate in Discontinuous Conduction Mode (DCM). This requires control circuits that accurately distribute the current in proportion to the voltage error of each output. However, it remains challenging to supply concentrated correction current in response to significant load fluctuations at a certain sub-converter output. As its countermeasure, SIMO converters that change the control order when large load fluctuations occur have also been proposed [7–13].

2.3. SIMO Converters with Exclusive Control Method

The third control method for the SIMO converters introduced in this review is with the exclusive control method, which involves supplying the current controlled by PWM pulse to the selected one sub-converter output

voltage each cycle. However, the control order for each sub-converter is entirely indefinite and not predetermined. At the end of each clock pulse, the control target sub-converter for the next cycle is exclusively determined. This is expected to result in simple implementation, fast response and small ripple. The error voltage amplification outputs of all sub-converters are compared using a wired-OR circuit, selecting the sub-converter having the largest error voltage as the control target for the next cycle. Simultaneously, the PWM pulse generated in the selected sub-converter is supplied to its power stage. The advantage of this method is that it always prioritizes the sub-converter having the largest error voltage; this means that it focuses on the one with the greatest output voltage ripple. Then the system can suppress voltage ripples more efficiently. This control method automatically selects the optimal sub-converter in response to the load variation conditions of each sub-converter; it minimizes the voltage ripple of the overall converter, and further it can realize the fast transient response [14–22].

Moreover, this control method is not only applicable to SIMO converters using fixed-frequency clock pulses, but it can also be easily applied to converters using control methods that do not utilize clock pulses, such as ripple control and soft-switching control methods. Further, it can be applied to multi-output SEPIC converters.

3. Fundamental DC-DC Switching Converters

There exist three types of fundamental DC-DC switching converters: buck, boost, and buck-boost converters. Their configurations are almost the same in terms of components in power and control stages. Each of their power stages is composed of a power switch, an inductor, a diode, and an output capacitor. Each control stage is also quite similar, consisting of a comparator, a flip-flop (FF), and a reference voltage source. The differences in converter configurations are distinguished by the positions of the switch, the diode, and the inductor. Additionally, the input-output voltage conversion ratio (Vo/Vi) and the polarity of Vo are different, where Vi and Vo denote the input voltage and the output voltage, respectively. Specifically, the input-output relationships are are as follows: $0 < Vo < Vi$ for the buck converter, $0 < Vo < Vi$ for the boost converter, and $0 < -Vo \gtrless Vi$ for the buck-boost converter.

3.1. Buck Converter with PWM Control

Figure 1 depicts the buck converter configuration. The red broken line represents the current flow when the PWM pulse level is either high or low. Figure 1 illustrates that the converter has two stages and comprises three main components.

- Power Stage: Composed of a power switch (SW), an inductor (L), a diode (Di), and a capacitor (Co).
- Control Stage: Composed of an amplifier (AMP), a comparator (Comp), an FF, and a sawtooth generator.

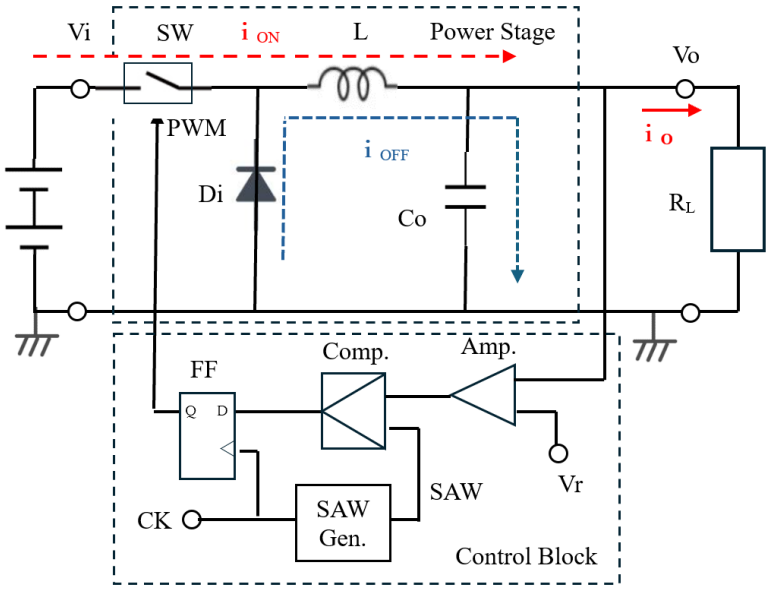


Figure 1. Buck converter configuration [21] ©IEEE.

Notably, the positions of SW, L, and Di are distinctive features of the buck converter.

In the power stage, SW is regulated by the PWM pulse. When it is high, SW turns ON, and the input current from the power supply flows through SW to L (as shown by the red broken line in Figure 1). During this period, the input current increases, flowing into Co and RL, increasing Vo (Figure 2) and raising the energy stored in L.

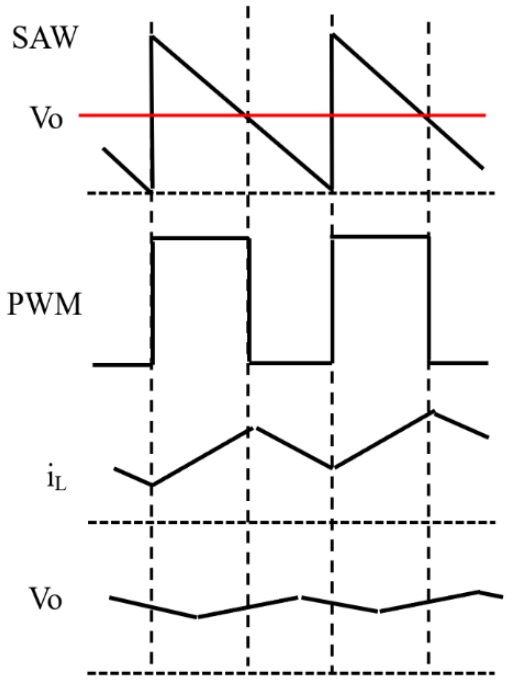


Figure 2. Timing diagram of Figure 1.

Conversely, in case the PWM level is low, SW turns off, and the energy in L causes current to flow through Di (as indicated by the blue dotted line in Figure 2). As a result, Vo decreases slightly. When Vo decreases, the duty ratio (D) of the PWM pulse increases.

In the control stage, AMP compares and amplifies the error of Vo from the reference Vr. This amplified error ΔVo is subsequently compared against the sawtooth signal (SAW) to produce the PWM signal. The FF receives this data synchronously with the internal clock pulse (CK) to provide the SAW signal, that is produced by the sawtooth generator. Vo varies depending on D as shown in Equation (1).

$$Vo = D \cdot Vi \tag{1}$$

Since $0 < D < 1$, we have $0 < Vo < Vi$.

3.2. Boost Converter and Buck-Boost Converter

Figure 3 illustrates the boost converter configuration. Its power stage consists of the same components as the buck converter, but their connections are different. Its control stage is similar to the buck converter. When SW is ON, the input current flows into L, but it does not flow to Co or RL (Figure 3). During this period, L charges the magnetic energy. When SW is off, L allows current to flow into Co and RL through Di. As a result, the current into Co is intermittently interrupted, leading to a larger voltage ripple for Vo compared to the buck converter. Vo is given by Equation (2):

$$Vo = 1/(1 - D) \cdot Vi \tag{2}$$

Since $0 < D < 1$, we have $1 < 1/(1 - D)$ and $Vo > Vi$.

The buck-boost converter provides a negative voltage output. Figure 4 illustrates the buck-boost converter configuration, where the connections among SW, Di, and L differ from the other two converters. Notably, the direction of Di is reversed. Here is how it operates:

- When SW is ON, the input current flows through SW and L (red dotted line).
- When SW is OFF, the inductor current flows into Co in a reverse direction (blue dotted line).

As a result, the polarity of Vo becomes negative, and Vo is expressed by Equation (3):

$$Vo = -D/(1 - D) \cdot Vi \tag{3}$$

Since $0 < D < 1$, the value of $D/(1 - D)$ varies, allowing the absolute value of Vo to exceed Vi.

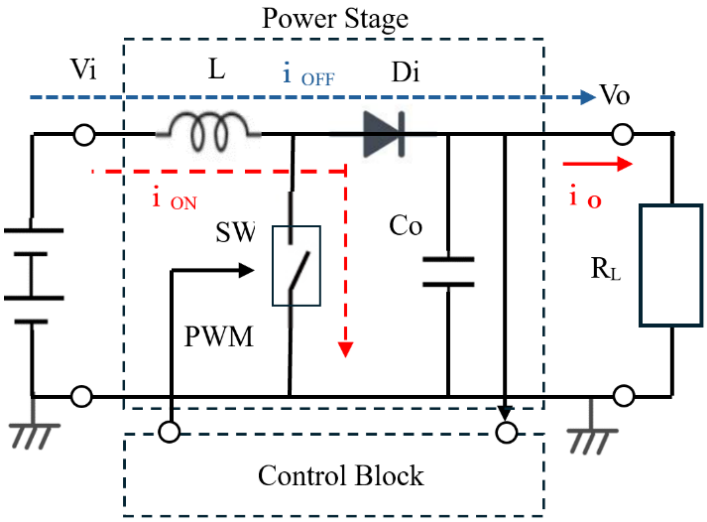


Figure 3. Boost converter configuration [21] ©IEEE.

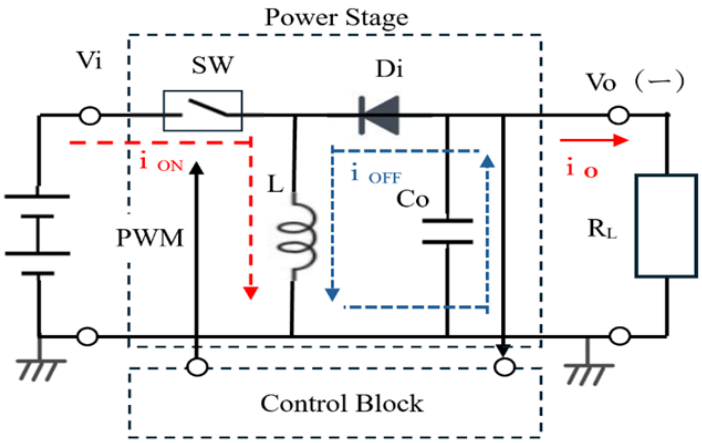


Figure 4. Buck-boost converter configuration [21] ©IEEE.

4. SIDO Converters with Exclusive Control Method

4.1. SIDO Buck-Buck Converter with PWM Control

4.1.1. Circuit Configuration and Operation

The SIDO buck-buck converter is depicted in Figures 5 and 6. There, the solid red line represents the current flow during inductor charge, while the dashed blue line illustrates the one during inductor discharge. Figures 5 and 6 illustrate the case when Converter 1 or 2 is regulated, respectively.

(1) In case Converter 1 is chosen, and V1 is regulated (Figures 5 and 7a).

- S2 remains consistently OFF.
- S0 is controlled by the PWM1 signal at 500 kHz.
- When PWM1 is high, S0 is ON, and L is charged.
- Subsequently, when PWM1 goes low, S0 turns off, and L is discharged through D0 and D1. During this period, Converter 2 remains uncharged, but its output current is provided from C2.

(2) In case Converter 2 is chosen (Figures 6 and 7b).

- S2 remains continuously ON.
- D1 is kept off due to V1 > V2.
- Converter 2 operates as a typical buck converter in Figure 1.

Notice that when Converter 2 is chosen, Converter 1 is not served, but its load current is provided from C1.

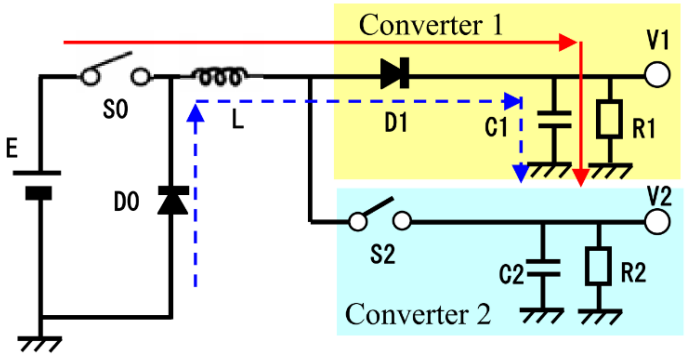


Figure 5. SIDO buck-buck converter when V1 is regulated [21] ©IEEE.

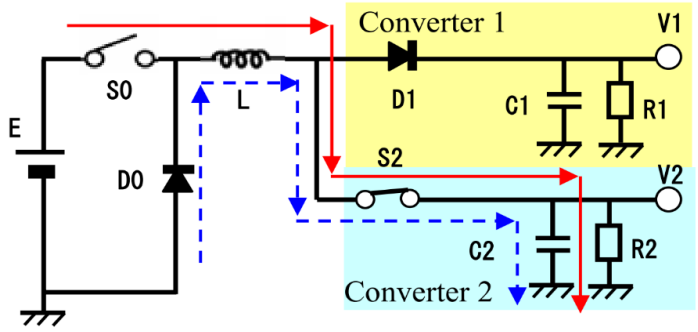


Figure 6. SIDO buck-buck converter when V2 is regulated [21] ©IEEE.

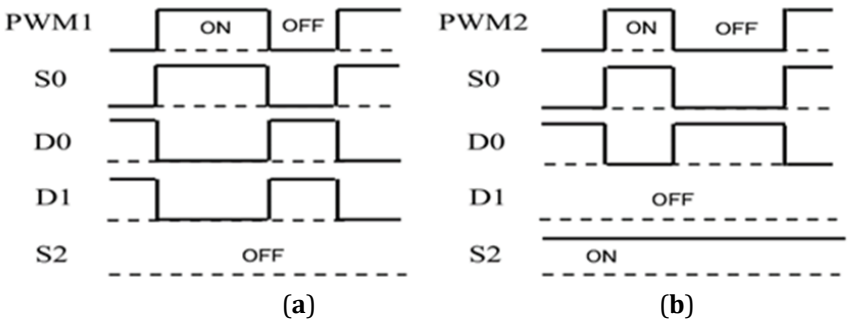


Figure 7. Timing diagram of switches in Figures 5 and 6 [21] ©IEEE. (**a**) Converter 1 control; (**b**) Converter 2 control.

4.1.2. Simulation Circuit and Results

The simulation circuit is depicted in Figure 8, while its timing diagram is in Figure 9. In this circuit, both the error amplifier outputs are compared by comparator 1 to choose ΔV1 or ΔV2. The selected error voltage is then compared by comparator 2 against a sawtooth wave SAW to produce a PWM signal. S0 and S2 are controlled by the PWM signal and the select signal, respectively.

In Figure 8, Converter 2 has S2, while Converter 1 has the diode D1 instead of a switch. In previous SIDO converters, Converter 1 usually has a switch instead of D1. In this case, a timing problem called "dead time" occurs, which is the required time interval between the serial measuring pulses. In the previous SIDO converter with two switches in each converter, the dead time is caused when the polarity of the select pulse is changed for the converters from comparator 1. For example, the two switches must not be "ON" at the same time because the electric charge of C1 would rush into C2 due to V1 > V2. Conversely, in case two switches are off simultaneously, the inductor current induces a very high voltage, which is undesirable. In the configuration of Figure 8, there is no "dead time" because there is only a single switch S2. When S2 turns on or off, D1 automatically turns off or on.

Table 1 shows the simulation conditions, and the converter operates in DCM (Figure 10). Peak currents are caused by the SEL signal change from Converter 1 to Converter 2 at t = 3.991 ms and 4.039 ms. Figure 11 shows the waveforms of V1, V2, I1 and I2.

Here, the transient response simulation results are obtained when I1 is varied from 1.0 A to 2.0 A and vice versa, and I2 is changed to 0.2 A, 1.2 A, and 2.2 A.

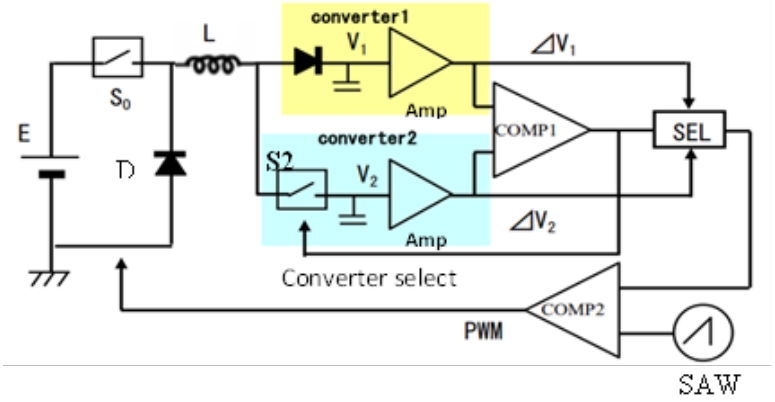


Figure 8. SIDO buck-buck converter configuration for simulation [21] ©IEEE.

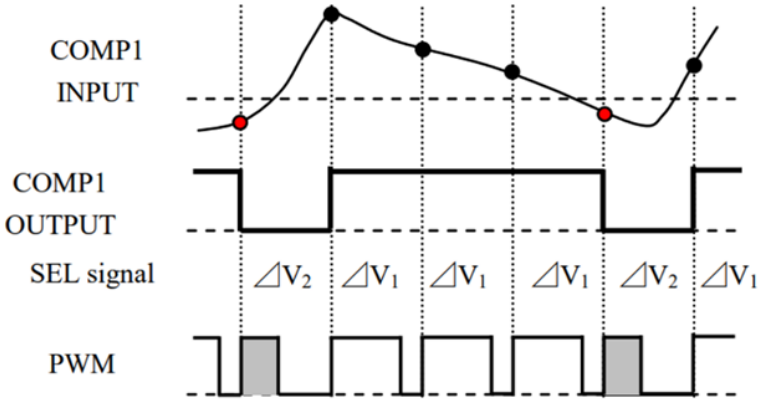


Figure 9. Timing diagram of Figure 8 [21] ©IEEE.

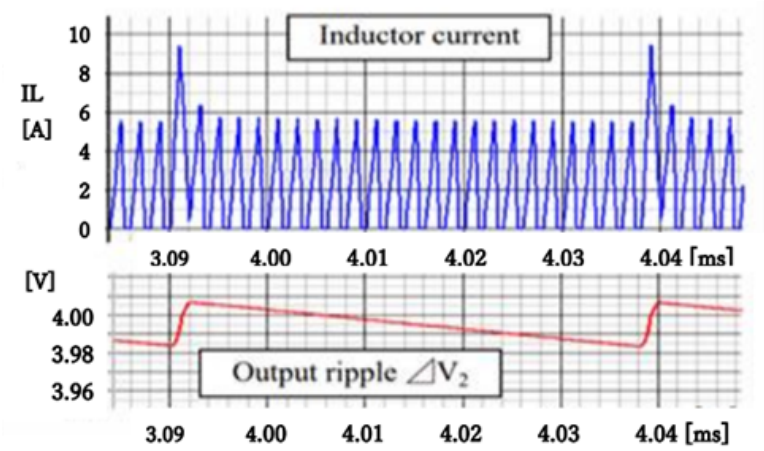


Figure 10. Simulated waveforms of IL and ΔV2 [21] ©IEEE.

Table 1. Simulation conditions of Figure 8.

Parameter	Value
E	9.0 V
L	0.5 µH
C	470 µF
$V1$	6.0 V
$V2$	4.0 V
Fck	500 kHz

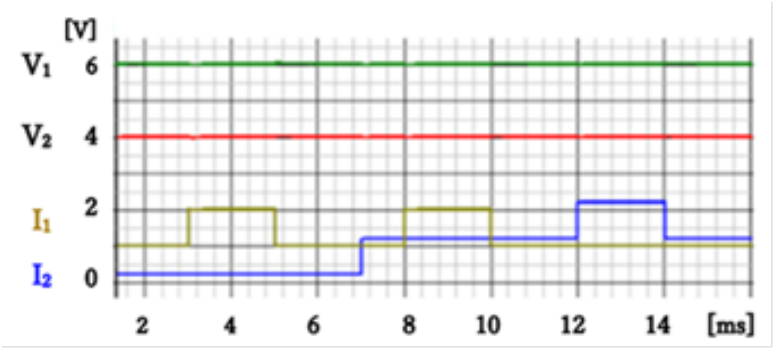


Figure 11. Waveforms of V1, V2, I1 and I2 [21] ©IEEE.

Figures 12 and 13 show the output ripples ΔV1, ΔV2 for (I1, I2) =(2 A, 0.2 A) and (I1, I2) = (1 A, 2.2 A). In Figure 12, I1 : I2 is 10 : 1, while the output ripples are ΔV1=11 mVpp and ΔV2=19 mVpp, which are smaller than 0.5% of V1, V2, respectively. There, Converter 1 is regulated for 46 µs (23 clock periods) whereas Converter 2 is for 2 µs (1 clock period). We observe that ΔV2 exhibits a linear slope; this is due to that no current is provided to Converter 2 there.

In Figure 13, Converters 1, 2 are nearly regulated in an alternating manner. Since I2 is bigger than I1, V2 is occasionally regulated for two successive clock cycles. Figure 14 displays the transient responses V1, V2 in response to changes of I1, I2. There, the red solid arrow indicates self-regulation, while the blue dashed arrow does cross-regulation. They typically exhibit nearly identical characteristics when they occur simultaneously.

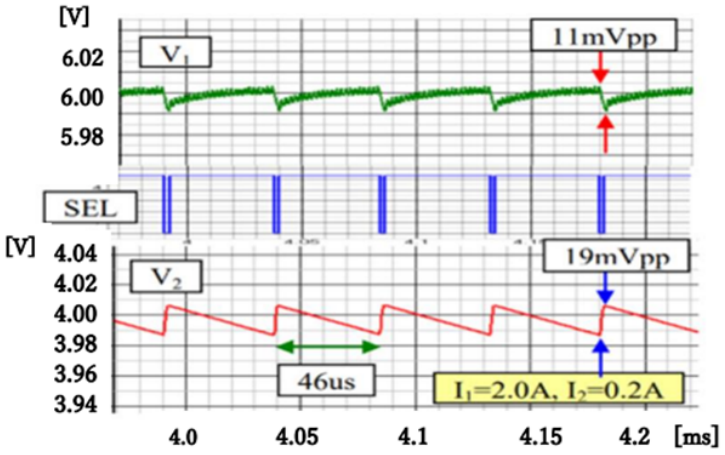


Figure 12. Output voltage ripples for I1 = 2.0 A, I2 = 0.2 A [21] ©IEEE.

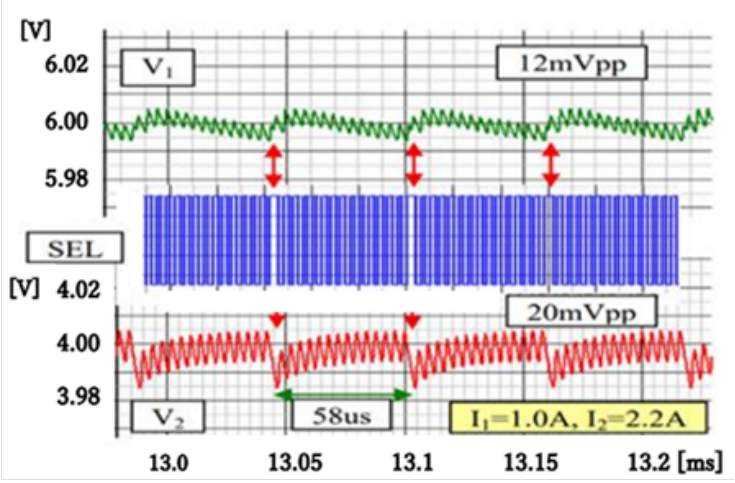


Figure 13. Output voltage ripples for I1 = 0.2 A, I2 = 2.0 A [21] ©IEEE.

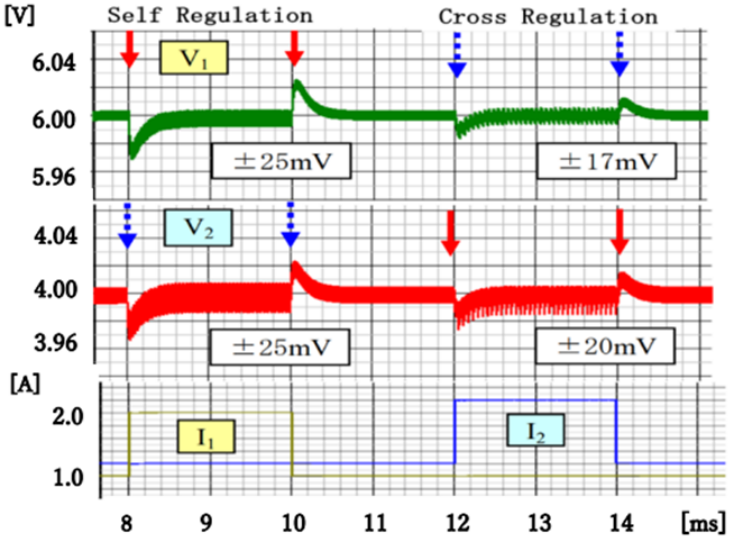


Figure 14. Transient responses of V1 and V2 [21] ©IEEE.

In this context, cross-regulation describes the overshoot caused by output current changes in another converter, whereas self-regulation pertains to the overshoot resulting from changes in the converter's own output current.

4.2. SIDO Boost-Boost Converter with PWM Control

4.2.1. Circuit Configuration and Operation

The SIDO converter with two boost converters is depicted in Figures 15 and 16. There, the solid red line indicates the current flow during the inductor charge, while the dashed blue line illustrates the one during its discharge. Figure 15 displays the case when Converter 1 is regulated, whereas Figure 16 does the one when Converter 2 is.

(1) In case Converter 1 is regulated (Figures 15 and 17a):

- S2 remains consistently OFF.
- S0 is controlled by PWM1 at 500 kHz.
- When PWM1 is high, S0 is ON, and L is charged.
- Subsequently, when PWM1 turns low, S0 turns off, and L is discharged. The inductura current flows into input voltage source E through D1
- Converter 2 remains uncharged, and its output current is provided from C2.

(2) In case Converter 2 is regulated (Figures 16 and 17b):

- S2 remains continuously ON, and D1 is off due to V1 > V2.
- Converter 2 operates as a typical boost converter in Figure 3.

The operation is similar to that in Figure 4, though its topology now involves a boost converter. Refer to Table 2 for the simulation conditions.

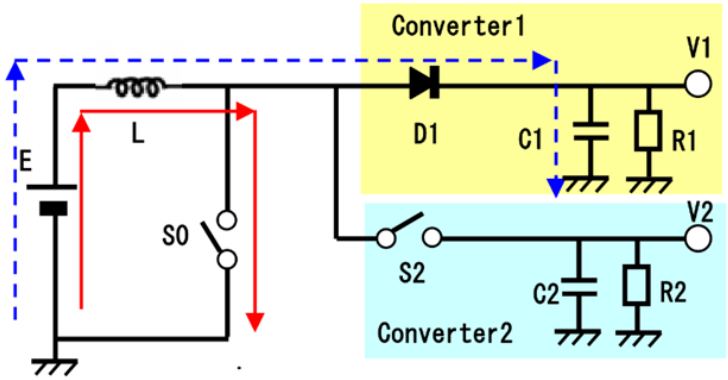


Figure 15. SIDO boost-boost converter when V1 is regulated [21] ©IEEE.

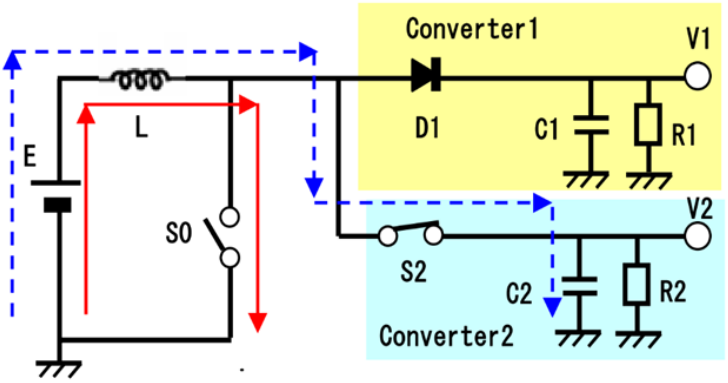


Figure 16. SIDO boost-boost converter when V2 is regulated [21] ©IEEE.

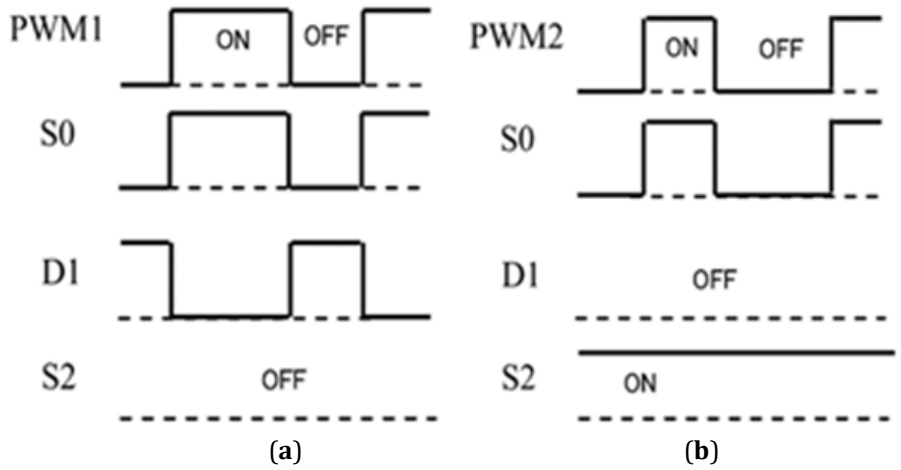


Figure 17. Timing diagram of switches and diode control [21] ©IEEE. (**a**) Converter 1 controlled; (**b**) Converter 2 controlled.

Table 2. Simulation Conditions of Figures 15 and 16.

Parameter	Value
E	3.0 V
L	0.5 µH
C	470 µF
$V1$	6.0 V
$V2$	4.0 V
Fck	500 kHz

4.2.2. Simulation Results

Figure 18 shows the simulated waveforms of V1, V2, I1 and I2. There, I1, I2 are set to 0.2 A, 1.2 A, and 2.2 A. Figures 19 and 20 illustrate the output voltage ripples ΔV1, ΔV2 for (I1, I2) = (2.0 A, 0.2 A) and (I1, I2) = (0.2 A, 2.0 A). I1 : I2 is 11 : 1, and the ripples are ΔV1 = 22 mVpp, ΔV2 = 15 mVpp, which are smaller than 0.4% of V1, V2, respectively.

Figure 21 displays the transient responses of V1, V2 for changes in I1, I2. The red solid arrow indicates self-regulation ripples which result in ΔV1 = 75 mVpp, ΔV2 = 40 mVpp, while the blue dashed arrow does cross-regulation ones which result in ΔV1 = 25mVpp, ΔV2 = 75 mVpp.

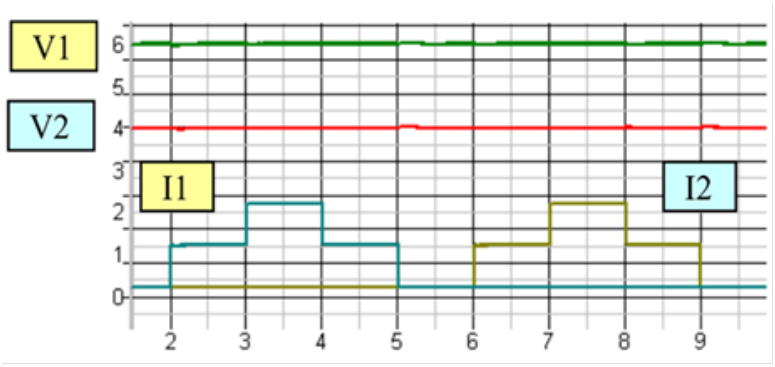


Figure 18. Waveforms of V1, V2, I1 and I2 [21] ©IEEE.

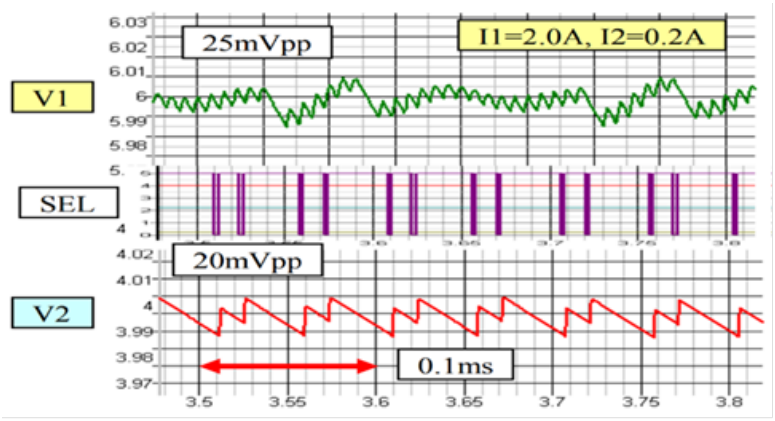


Figure 19. Output voltage ripples for I1 = 2.0 A, I2 = 0.2 A [20] ©IEEE.

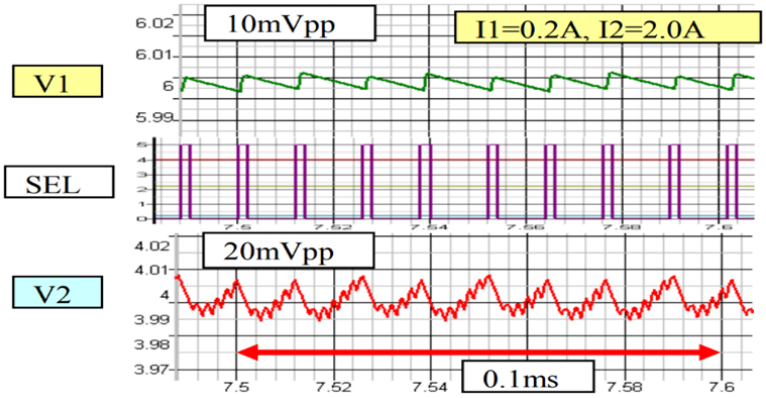


Figure 20. Output voltage ripples for I1 = 0.2 A, I2 = 2.0 A [21] ©IEEE.

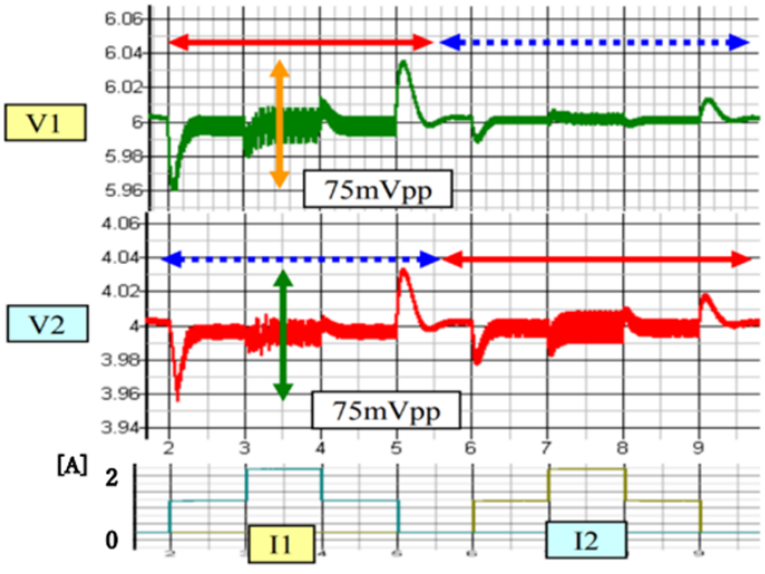


Figure 21. Transient responses of V1 and V2 [21] ©IEEE.

4.3. Experimental Results of SIDO Converters with PWM Control

4.3.1. Load Regulations of SIDO Buck-Buck Converter

Figure 22 shows the measured output voltages of the SIDO buck-buck converters for Vi = 9.0V. There, the outputs are V1 = 5.98 V and V2 = 4.54 V, whereas the references are V1ref = 6.2 V and V2ref = 4.5 V. We observe a small offset of 0.2 V for V1; it is probably due to improper phase lag compensation.

Figure 23 illustrates the self-regulation of Converter 2 and the cross-regulation of Converter 1 for I2 change from 0.36 A to 0.60 A or vice versa. They exhibit an offset of about 5 mVpp. Figure 24 provides an enlarged view of Figure 19. We observe that their overshoots are approximately 5 mVop; the response characteristics of this converter are good.

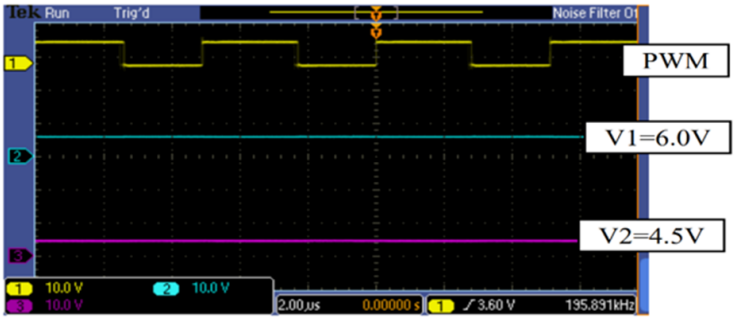


Figure 22. Output voltages of SIDO buck-buck converter [21] ©IEEE.

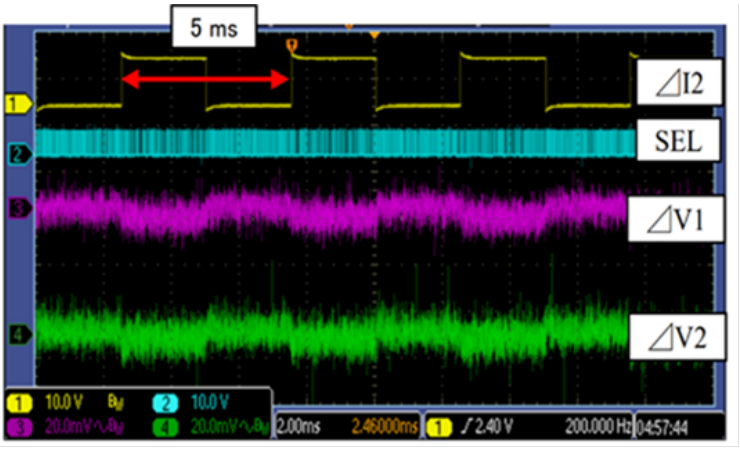


Figure 23. Transient regulations of SIDO buck-buck converter for ⊿I2 [21] ©IEEE.

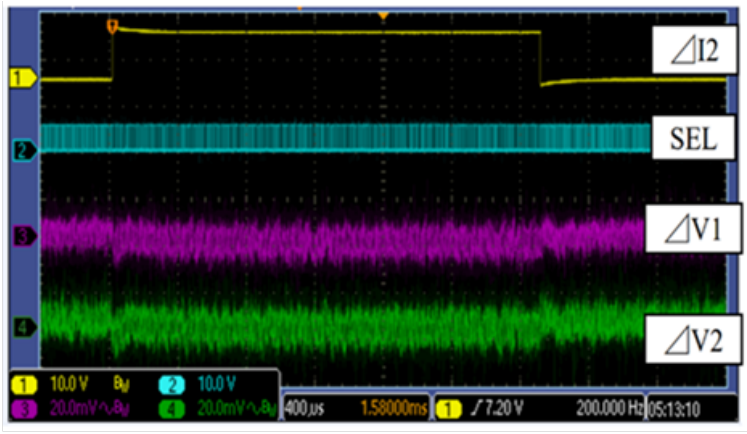


Figure 24. Enlarged transient regulations of SIDO buck-buck converter [21] ©IEEE.

4.3.2. Load Regulations of SIDO Boost-Boost Converter

Figure 25 displays the measured waveforms of our SIDO boost-boost converters. We notice slight noises in the output voltages, roughly 20mVpp; these are likely due to the circuit being built on a universal board. Implementing our converters on a printed circuit board could reduce these noises.

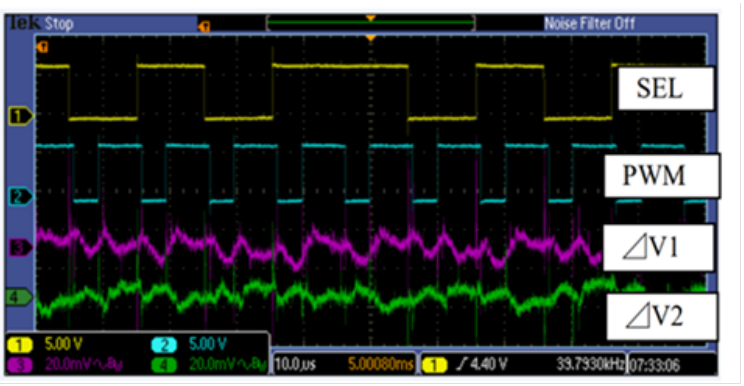


Figure 25. Output voltages of SIDO boost-boost converter [21] ©IEEE.

Figures 26 and 27 show the self- and cross-regulations. Figure 26 illustrates the self-regulation of V1 and the cross-regulation of V2 for I1 change from 0.09 A to 0.18 A. Figure 27 shows the cross-regulation of V1 and the self-regulation of V2 for I2 change from 0.11 A to 0.22 A. The self- and cross-regulations are smaller than 5mV for both outputs.

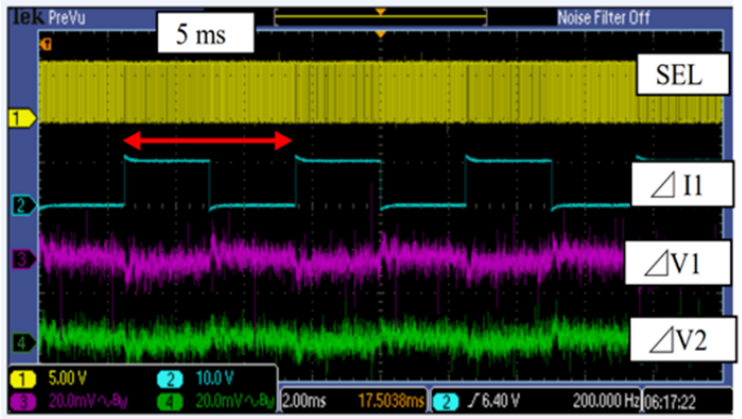


Figure 26. Transient regulations of SIDO boost-boost converter for ⊿I1 change [21] ©IEEE.

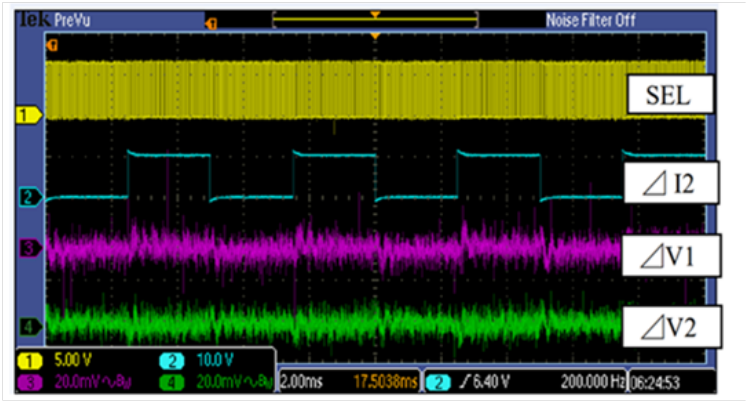


Figure 27. Transient regulations of SIDO boost-boost converter for ⊿I2 change [21] ©IEEE.

Figure 28 provides an enlarged view of Figure 27. We observe that the responses of V1, V2 exhibit slight oscillations for 2 or 3 periods, and their overshoots are roughly 5 mVop. The periods of the oscillations are approximately 330 μs, and the cutoff frequency is approximately 3 kHz; these would be appropriate for the converter built on a universal board using discrete components.

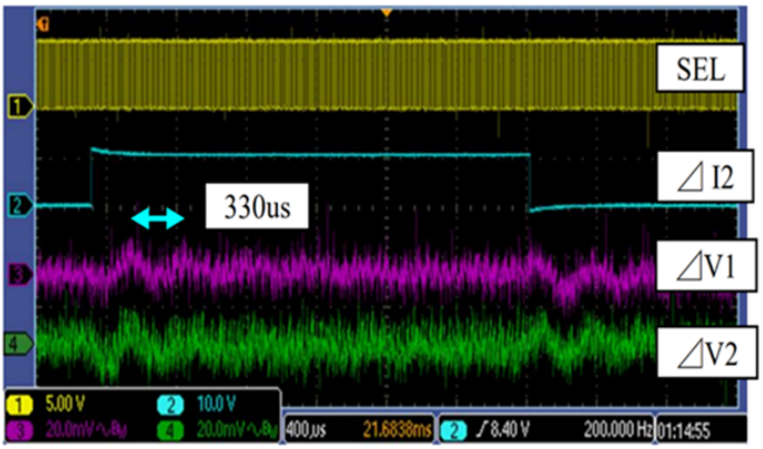


Figure 28. Enlarged transient regulations of SIDO boost-boost converter [21] ©IEEE.

Remarks:

(i) The ripple noise in the output current during steady-state operation appears as a ratio of the output voltage Vo and the output voltage ripple ⊿Vo included in it. ⊿Vo is independent of Vo and is primarily related to the switching frequency Fc, the inductor L, the output capacitor Co, and the output current Io. It is represented by the equation $\Delta Vr \propto Io / (Fc\ L\ Co)$.

For example, in the case of Figure 10 to Figure 14, given Vo = 4V and Io = 2A, ⊿Vo = 20mVpp. Thus, for the output current Io display, the current ratio is ⊿Io/Io = 20mV/4V = 10mA/2A = 0.005. Consequently, the noise display in the current graph is 0.5%, which is very small. Visually, it appears as a clean waveform with minimal noise.

(ii) Notice that there are discrepancies between actual results and simulations regarding output voltage ripple. The steady-state output voltage ripple is represented by the formula $\Delta Vr \propto Io/FcLCo$, as mentioned above. However, in real circuits, the following factors also come into play:

1. Output Capacitor Internal Resistance ESR (Equivalent Series Resistance):

   A real capacitor has internal resistance. For a 100μF capacitor, the ESR for an electrolytic capacitor is approximately 50 mΩ. For the recent multilayer ceramic capacitors, at Fc=0.5 MHz, the ESR is approximately 3.2 mΩ, based on the calculation formula: $ESR \fallingdotseq 0.16 / (F * C)$.

2. Also, some noises are superimposed by the GND line, even though noises superimposed by crosstalk between wiring are minimal in the power line.

5. SIDO Hysteretic Converter with Ripple-Based Control

5.1. Basic Buck-Type Hysteretic Converter

5.1.1. Circuit and Operation

Figure 29 depicts the configuration of a basic buck-type hysteretic converter with the ripple-based control. It is composed of a power stage and a comparator, but no amplifier. Vo is directly compared against Vref. Figure 30 illustrates the timing diagram. In case Vo < Vref, the comparator output (CONT) becomes high after a slight delay. It turns SW on, and the current starts to flow from Vi into C and R through L after a delay Tdon from time B. When Vo becomes larger than Vref at time C, CONT becomes low and SW turns off after a slight delay, causing Vo to be slightly overcharged. The inductor current starts to decrease after a delay Tdoff at time D, and it flows also through the diode.

5.1.2. Relationship between the Output Ripple and the Control Signal

The rising inductor current ILR(t) from the time B to D is given by Equation (4):

$$I_{LR}(t) = (Vi - Vo) \cdot t / L \tag{4}$$

The peak current ID at time D is obtained using on-time TON from B to D as shown in Equation (5):

$$I_D = I_{LR}\, T_{ON} = (Vi - Vo)\, T_{ON} / L \tag{5}$$

The falling current ILF(t) and the falling time TF from D to E are expressed by Equations (6), (7):

$$I_{LF}(t) = ID - Vo \cdot t / L \tag{6}$$

$$I_{LF}(T_F) = (Vi - Vo)\, T_{ON} / L - Vo \cdot T_F / L = 0 \tag{7}$$

From Equations (6) and (7), we have Equation (8):

$$T_F = (Vi / Vo - 1)\, T_{ON} \tag{8}$$

Notice that L is typically about 1 μH for the overcharge minimization.

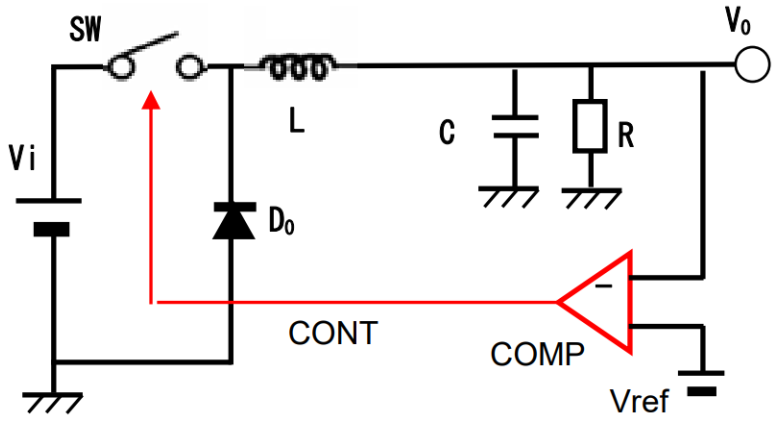


Figure 29. Basic hysteretic converter circuit.

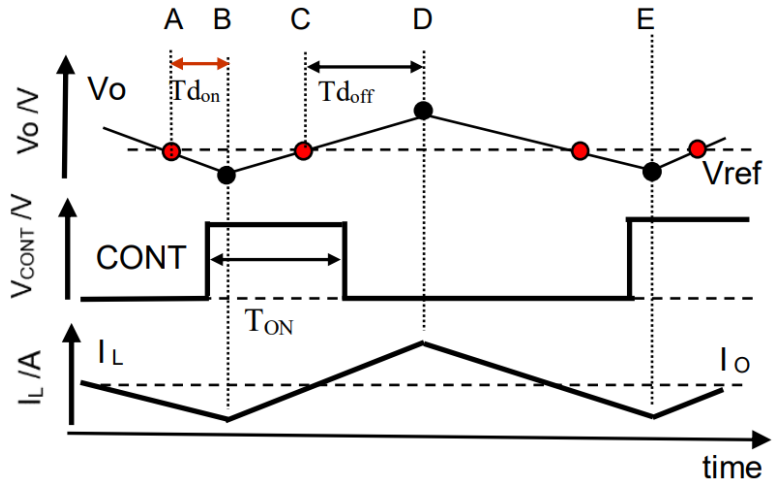


Figure 30. Timing diagram of basic hysteretic converter.

5.1.3. Simulation Results

Figure 31 displays the simulated ΔVo for an output current step ΔIo = 0.5 A of this hysteretic converter with conditions in Table 3. It responds quickly to load changes, resulting in only very small voltage ripple; it is smaller than 3 mVpp at Io = 0.5 A and about 7 mVpp at Io = 1.0 A (Figure 31). The overshoot is approximately 1 mV for the output current step of 0.5 A.

However, the basic hysteretic converter has several drawbacks. Firstly, ΔVo grows as Io increases (Figure 31). Secondly, the operating frequency may become very high and it varies depending on the load current, which may lead to significant EMI noise. Figure 31 shows that the frequency exceeds 150 kHz when Io = 0.5 A. Thirdly, the loop gain is relatively low due to no usage of an amplifier (Figure 29). This low loop gain causes an offset for Vo. Lastly, this hysteretic converter requires a little amount of voltage ripple for proper operation. Notice that its detection is difficult when ceramic capacitors are used instead of aluminum electrolytic capacitors.

Table 3. Simulation conditions of hysteretic converter.

Parameter	Value
Vi	9.0 V
L	1.0 µH
C	470 µF
Vo	5.0 V
Io	1.0/0.5 A

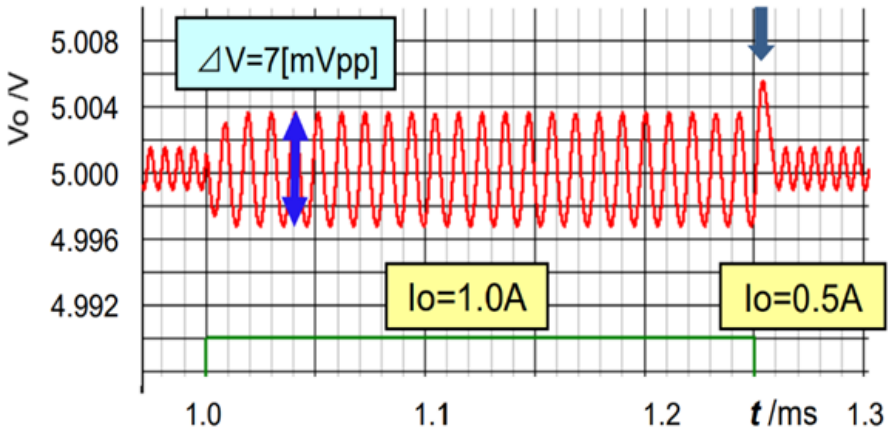


Figure 31. Output ripple of the basic hysteretic converter [16] ©JTSS.

5.2. Basic Hysteretic Converter with Triangular Signal

An RC network across the inductor generates a triangular signal for the ripple amplification and detection by the comparator (Figure 32). The RC network and an amplifier are added to the basic hysteretic converter in Figure 29. The RC network integrates the inductor voltage over time and produces a triangular signal bigger than the output voltage ripple. The regulation frequency varies based on the time constant RT CT, Io, and the hysteresis voltage of the comparator. Here, RT = 470kΩ and CT = 1.0nF. The amplified error of the output voltage from the reference voltage is compared against the triangular signal for the PWM signal generation, and it controls SW for the regulation of Vo.

Figure 33 shows the simulated waveforms of the output ripple in response to the output current change. The voltage ripple is about 5 mVpp at Io = 1.0 A at steady state, and the over/undershoots are about ±4 mV for Io change from 0.5 A to 1.0 A and vice versa. The regulation frequency is approximately 360 kHz.

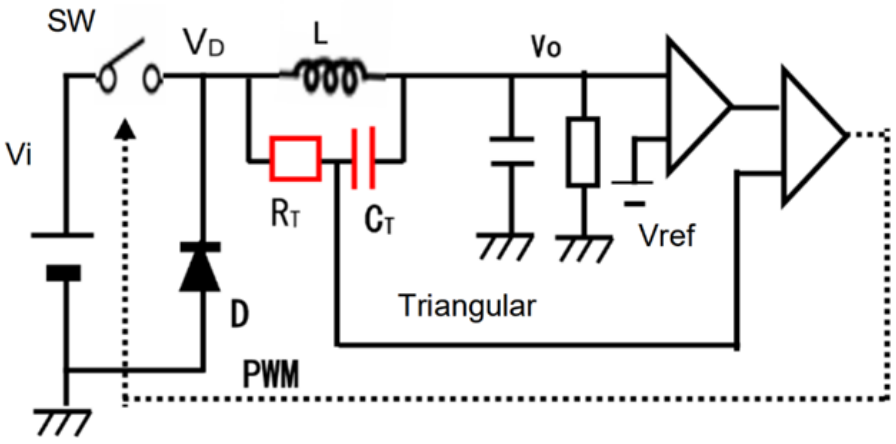


Figure 32. Configuration of the basic hysteretic converter with a triangular signal [16] ©JTSS.

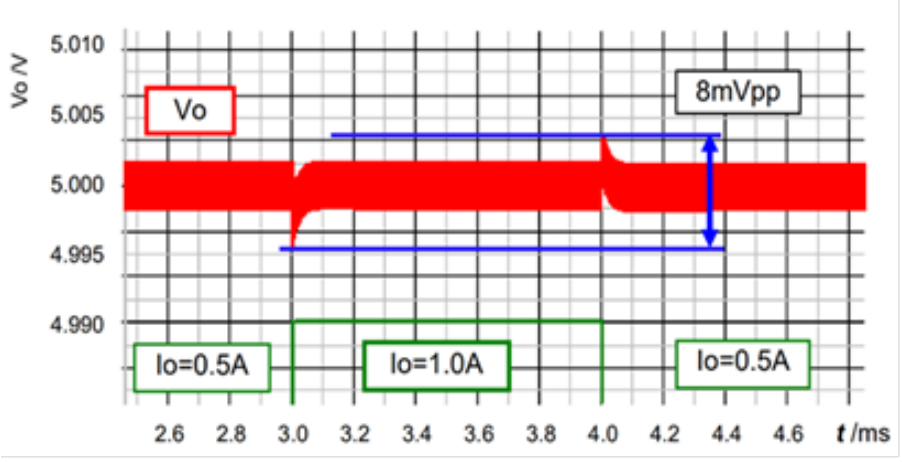


Figure 33. Simulated transient response of the basic hysteretic converter [16] ©JTSS.

5.3. SIDO Converter with Hysteretic Control

Figure 34 depicts the SIDO buck-buck converter with the hysteretic control using the triangular signal across the inductor. It is composed of a main power stage, an RC network, two buck sub-converters, a comparator, a switch (SW) to choose the PWM signal. One of two sub-converters is selected by the SEL signal, based on which has the larger error voltage ΔVo. The PWM signal (PWM1 or PWM2) is selected by the SEL signal.

Notice that the RC network generates a triangular signal synchronized with the PWM signal. One terminal of the RC network is connected to Vo1; this is because the voltage at the output terminal of the inductor changes based on the SEL signal. C has to be connected to a stable voltage terminal, such as Vo1, Vo2. This triangular signal is provided to two comparators in sub-converters for PWM1 and PWM2 generation. Here, Vi = 10 V, V1 = 5.0 V, V2 = 4.5 V, L=1.0 µH, and C=470 µF. Also, the operating frequency is approximately 500 kHz.

The switch in sub-converter 1 is virtually realized with a diode (Figure 34). In case the SEL signal is high, SW2 is ON, and sub-converter 2 is selected while the diode in sub-converter 1 is OFF. Here, Vo1 is set to be higher than Vo2. On the other hand, in case the SEL signal is low, SW2 is OFF, and hence sub-converter 1 is active.

Figure 35 shows the simulated output voltages. The ripples are about 2 mVpp at steady-state for I1=I2 = 0.5 A. The over/under-shoots are smaller than 10 mV for output current steps of ±0.5 A. Here, the time constant RC is approximately 4 ms.

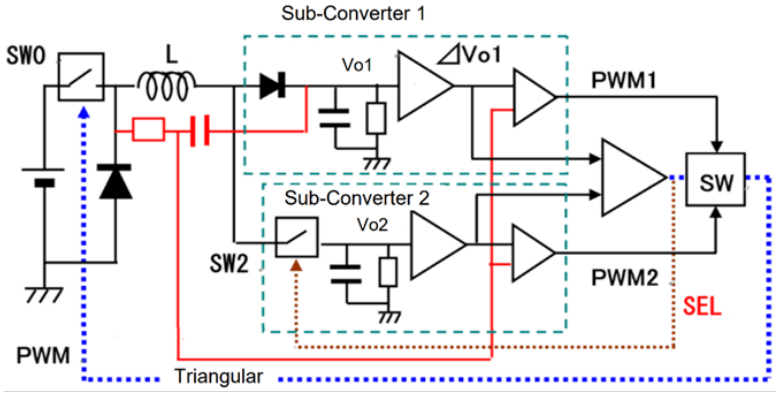


Figure 34. SIDO converter with the hysteretic control [16] ©JTSS.

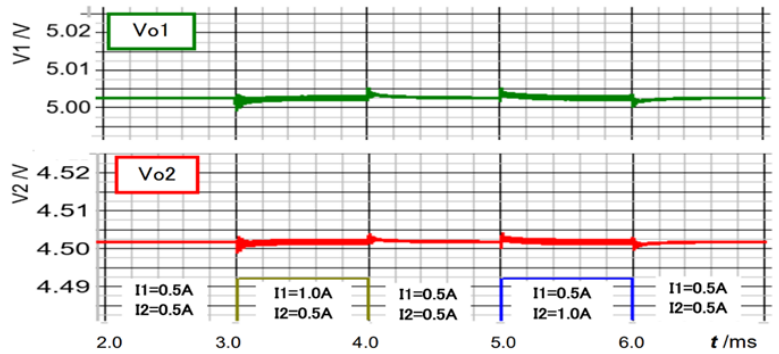


Figure 35. Simulated transient responses of the SIDO hysteretic converter [16] ©JTSS.

5.4. Experimental Results of SIDO Hysteretic Converter

Figures 36, 37, and 38 display the measured waveforms of the SIDO hysteretic converter using the conditions in Table 4. Figure 36 shows two output voltages, and we observe large spike noises of approximately 200 350 mVpp. Since the converter is fabricated on a universal board using discrete components, the impedance of the ground lines is high. Switching signals may cause noise in the ground lines or signal wires. The measured voltage ripples, excluding these spike noises, are about 50 mVpp, which are much bigger than the simulation results. In experiments, the operating frequency (Fop) is set low, around 60 kHz. Notice that the amplitude of the ripples in the buck converter is inversely proportional to Fop squared. In simulation it is 500 kHz, and the frequency ratio between the simulation and the measurement conditions is about 8. Therefore, the measured ripple amplitude in the experiment is reasonable. I1 is changed in 0.2 A step, and both the cross-regulation and self-regulation are minimal (Figure 36).

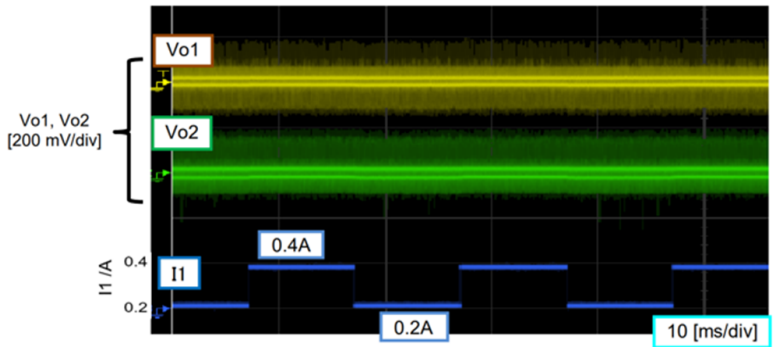


Figure 36. Measured output voltages of SIDO hysteretic converter [16] ©JTSS.

Figure 37 shows the measured waveforms of the SIDO hysteretic converter: the voltage VL across the inductor, the SEL signal, the PWM signal, and the triangular signal. Off-timing of the PMOS switch is significantly delayed. Also, the triangular signal amplitude is approximately 4 Vpp. The SEL signal duty ratio is nearly 50% due to the good balance of two output currents. The currents to the sub-converters are clearly divided by SEL (Figure 38). I1 flows when SEL is low and SW2 is off.

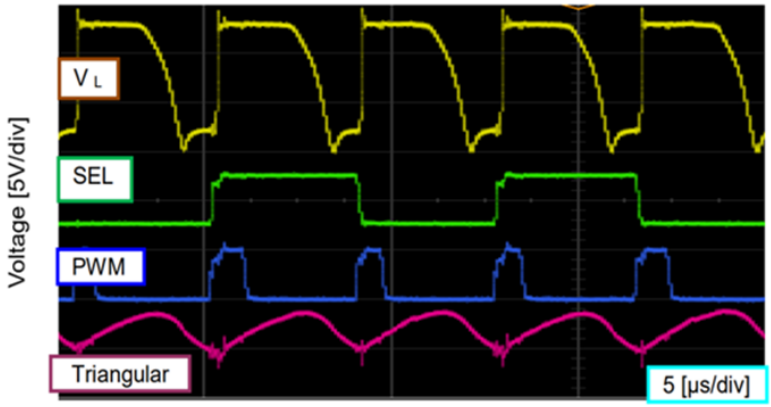


Figure 37. Measured waveforms of SIDO hysteretic converter [16] ©JTSS.

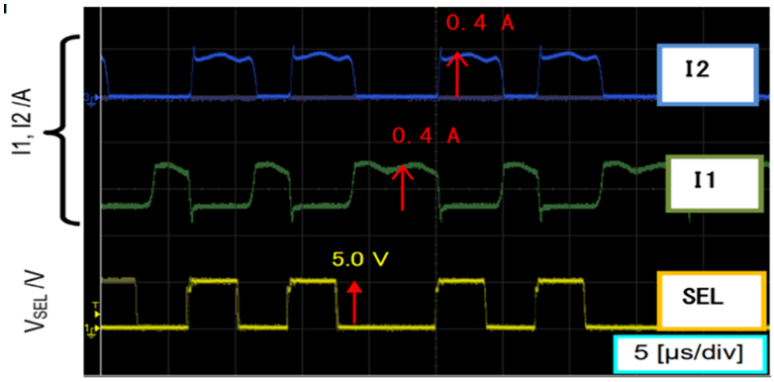


Figure 38. Measured waveforms of SIDO hysteretic converter [16] ©JTSS.

Table 4. Simulation conditions of SIDO hysteretic converter.

Parameter	Value
E	10 V
$V1$	5.0 V
$V2$	4.5 V
$I1$	0.2 A
$I2$	0.2 A
L	10 μH
Co	1,000 μF
R	4.0 kΩ
C	1.0 nF
Fck	60 kHz

6. Resonant SIDO Buck-Buck Converter with ZVS-PWM Control

6.1. Basic ZVS-PWM Controlled Resonant Buck Converter

Figure 39 illustrates the basic ZVS-PWM buck converter with half-resonant control. This converter incorporates Cr and a ZVS detection comparator into the fundamental buck converter. Cr is connected in parallel with the diode. The ZVS detection comparator compares the voltages Vsw and Vin. Figure 40 presents the simulated waveforms at steady-state of the converter. When Vsw exceeds Vin at the start of State 1, the ZVS detection comparator output goes high, setting an FF to the SET state; this high signal turns on M1. Consequently, M1 remains on, and the inductor current increases (Figure 40). Subsequently, the output voltage Vo surpasses Vref, and the amplified error voltage is compared against SAW. As Vo increases, the amplifier output decreases. Then, the PWM comparator output goes high, resetting the FF and causing its output to go low at State 2. Its operation is as follows (see Figure 40):

State 1: When the PWM signal is high, M1 turns on, and Vsw becomes equal to Vin. IL grows at a rate of (Vin - Vo) / L, and Cr is charged to Vin.

State 2: When PWM is low, M1 turns off, and D1 also turns off. IL is provided to the output by Cr, which was charged at State 1. Vsw gradually decreases due to the current drawn by Cr. Eventually, Vsw drops to a negative voltage until D1 turns on.

State 3: When Vsw is negative, D1 turns on. Then IL flows through the diode to ground, and IL decreases at a rate of Vo / L. Cr is discharged to a negative voltage equal to the forward bias voltage of D1.

State 4: When IL is negative, D1 turns off. IL flows from Co to Cr, causing Vsw to gradually increase from a negative voltage (approximately -0.7 V) to a positive voltage as it supplies current to Cr. When Vsw reaches Vin, the ZVS detection comparator output becomes high, turning M1 on and returning to State 1.

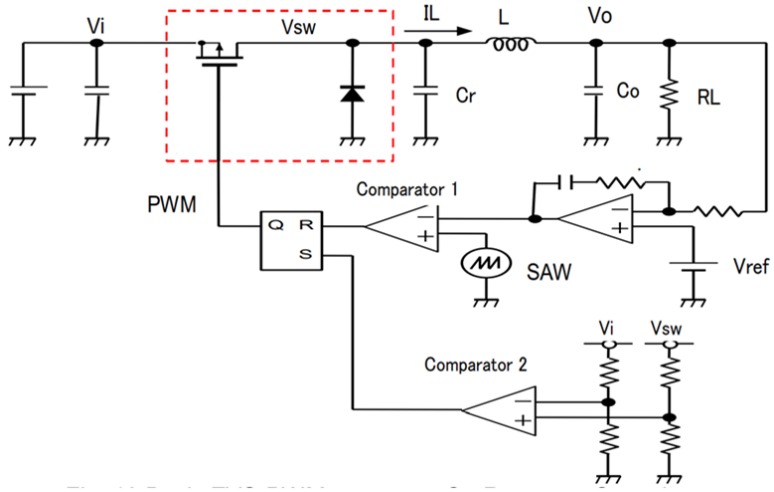


Figure 39. Basic VZS-PWM buck converter [16] ©JTSS.

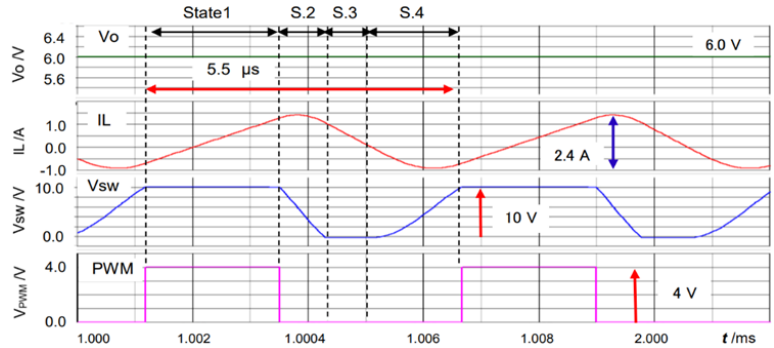


Figure 40. Simulated waveforms of basic ZVS-PWM converter [16] ©JTSS.

Figure 41 displays the experimental waveforms of the converter. A resonant switching converter is well known for its minimal switching losses. There, M1 turns ON when Vin=Vsw (Figure 40). This means that the voltage across M1 is zero, resulting in no switching loss. When M1 turns off, Cr keeps Vsw=Vin. Consequently, switching losses are significantly reduced due to the ZVS operation. Table 5 lists the simulation conditions.

Figure 42 displays the measured waveforms of the voltage (Vsw) across the switch and the current (Isw) through the switch. Figure 42a shows the waveforms in the fundamental buck converter, while Figure 42b shows those in the ZVS-PWM buck converter when the switch turns off. In the fundamental buck converter, there is considerable overlap between Vsw and Isw, causing switching losses. On the other hand, in the ZVS-PWM converter, there is no overlap.

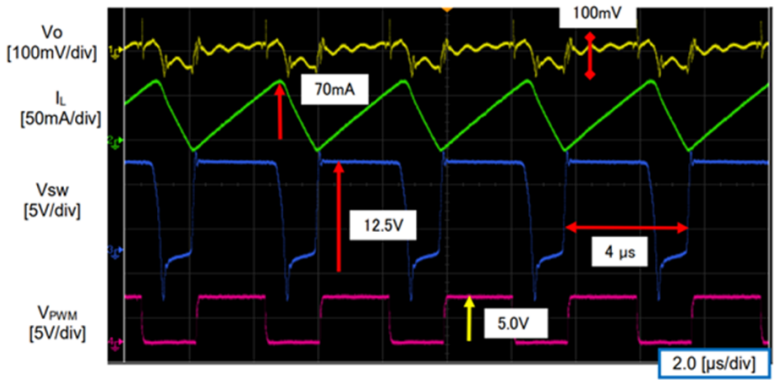
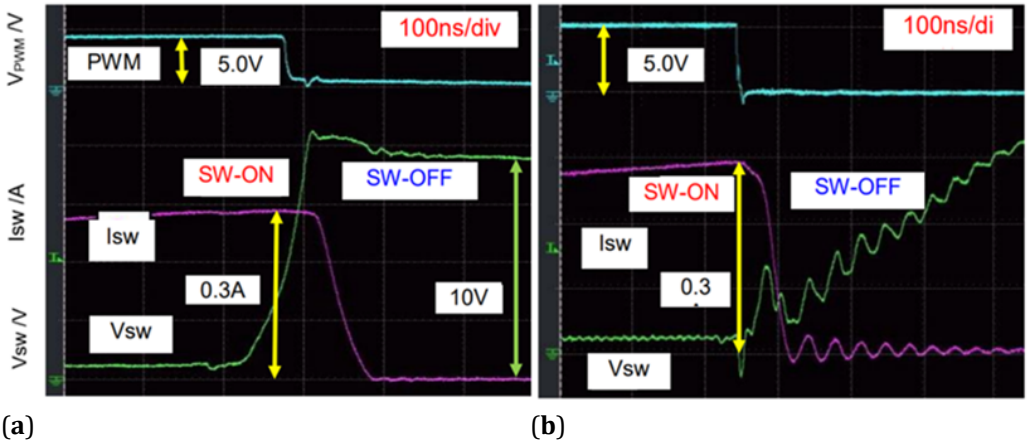


Figure 41. Measured waveforms of ZVS-PWM converter [16] ©JTSS.

Table 5. Conditions of ZVS-PWM converter.

Parameter	Value
Vin	10.0 V
Vo	6.0 V
L	1.0 µH
Cr	47 nF
Co	470 µF
Io	0.30 A



(**a**) (**b**)

Figure 42. Comparison of measured waveforms of voltages and currents across the switch [16] ©JTSS. (**a**) Fundamental PWM buck converter; (**b**) ZVS-PWM buck converter.

6.2. SIDO Buck-Buck Converter with ZVS-PWM Control

Figure 43 illustrates the SIDO buck-buck converter with ZVS-PWM control [8], while Figure 44 presents its simulated steady-state waveforms under the conditions in Table 6. The SIDO ZVS-PWM converter comprises one power stage with a resonant capacitor (Cr), two sub-converters, each equipped with an amplifier and a comparator, and a control stage that employs two FFs and a comparator. The SEL signal is generated by comparing ΔVo1 and ΔVo2 to decide whether the inductor current is provided to Vo1 or Vo2; Vo1 is selected when ΔVo1 > ΔVo2. This is referred to as "exclusive control." The ZVS signal detection and the subsequent turning on of M1 mark the timing for this control.

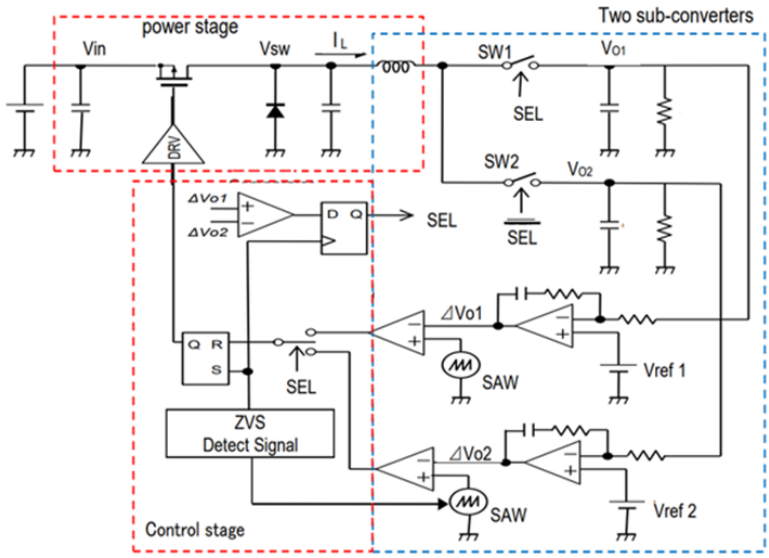


Figure 43. Configuration of SIDO ZVS-PWM buck-buck converter [16] ©JTSS.

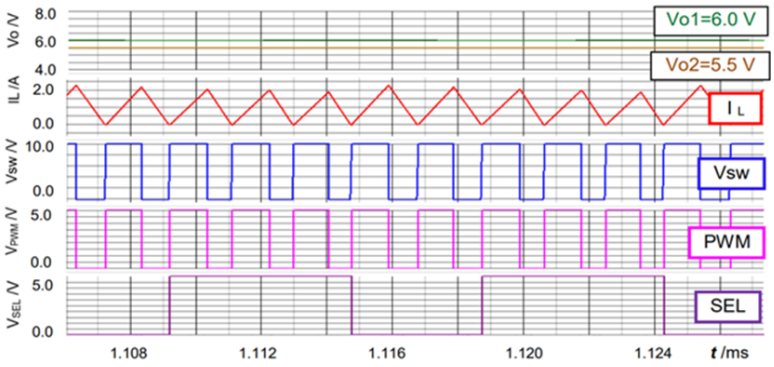


Figure 44. Simulation waveforms of SIDO ZVS-PWM buck-buck converter [16] ©JTSS.

Figure 45 shows the transient responses of the output voltages for the output current change by ±0.5 A of I1=1.0 A and I2=0.5 A, or vice versa. Both the self-regulation and cross-regulation are within ±15 mV, which are smaller than ±0.3% of Vo1 and Vo2. These are satisfactory for many applications.

The above simulation uses ideal switches. However, the experimental circuit uses MOSFET switches and they have an internal body diode (Figure 46a). This issue has been encountered also in other SIDO converters, but it can be solved by replacing the upper MOS switch (SW1) with a diode (Figure 46b). However, in this SIDO ZVS-PWM converter, this solution introduces another problem: reverse current from Co1 to Cr in case sub-converter 1 is selected.

This problem can be solved by ensuring that in case sub-converter 1 is selected, the reverse current is always

supplied from Co2 to Cr (Figure 46b). There, V2 is set smaller than V1. Figure 47 displays the simulated waveforms of Figure 46b, with yellow arrows indicating the period of the reverse current flow and the SW2 activation. Figure 48 shows the measured waveforms of output voltages and associated signals, with output voltage ripples around 40 mV, including spike noises.

Table 6. Conditions of SIDO ZVS-PWM converter.

Parameter	Value
Vin	10.0 V
$Vo1$	6.0 V
$Vo2$	5.5 V
L	2.2 µH
Cr	1.0 µF
$Co1$	470 µF
$Co2$	470 µF

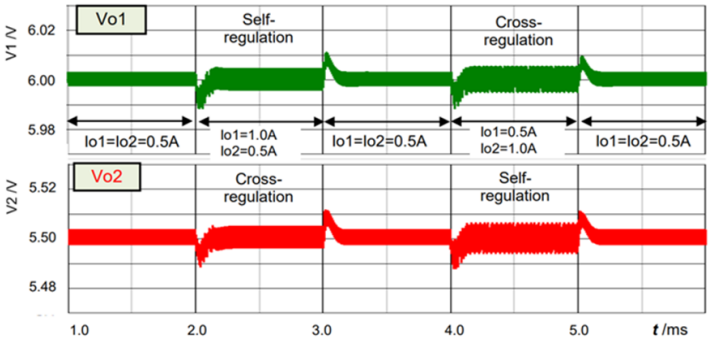


Figure 45. Simulated transient responses of SIDO ZVS-PWM converter [16] ©JTSS.

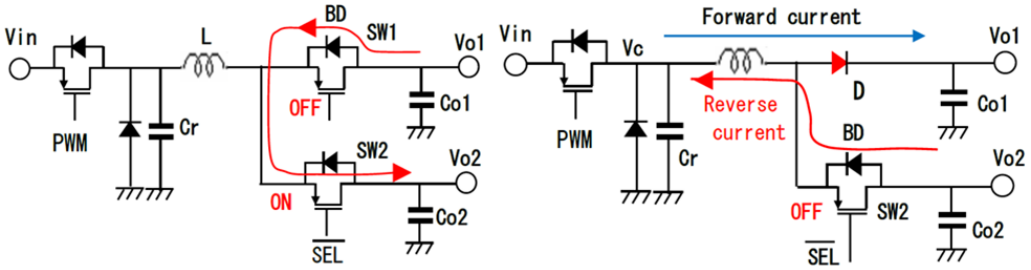


Figure 46. SIDO ZVS-PWM converter with solution for reverse current of body diode [15] @JTSS (**a**) Problem with an upper MOS switch (SW1); (**b**) Solution using a diode (D) when converter V1 is selected.

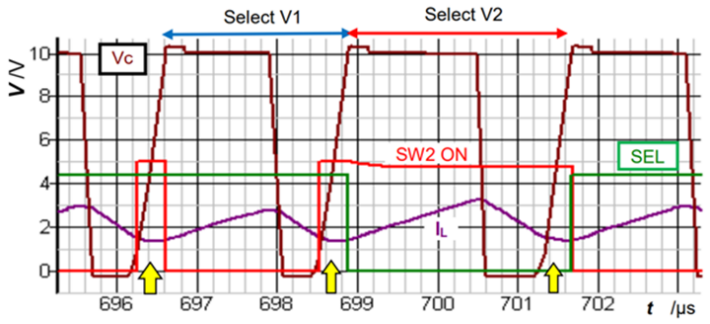


Figure 47. Simulated waveforms of improved SIDO ZVS-PWM converter [16] ©JTSS.

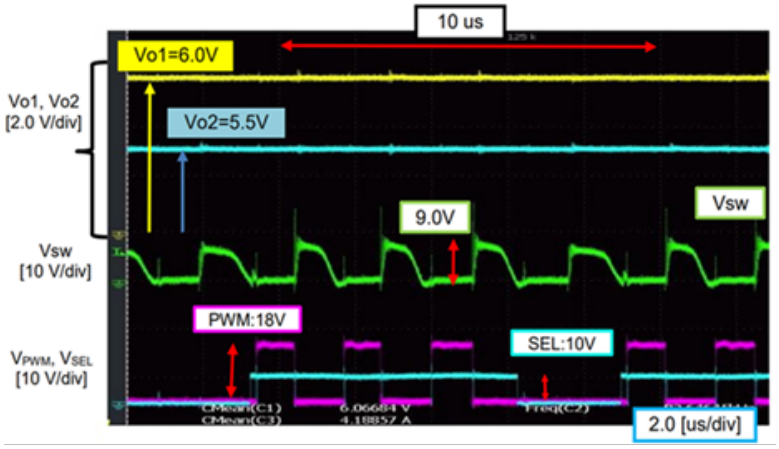


Figure 48. Measured waveforms of improved SIDO ZVS-PWM converter [16] ©JTSS.

7. Soft-switching SIDO Converter with Voltage Resonance

7.1. Basic Soft-Switching Converter with Half-Wave Voltage

Figure 49 illustrates the basic soft-switching converter with half-wave voltage resonance. It comprises a power stage and a control stage, as well as a load resistor. The power stage includes a main switch (SW) with its body diode (Db), an inductor (Lo), an output capacitor (Co), a free-wheel diode (Do), a resonant inductance (Lr), and a resonant capacitor (Cr). The control stage is composed of a saw-tooth generator, an error amplifier, and two comparators. Comparator 1 produces the PWM signal by comparing the amplified error voltage with the saw-tooth signal (SAW). Comparator 2 compares the resonant voltage (Vr) against the diode voltage (Vd) to monitor the voltage across SW and generate the trigger pulse for the SAW signal.

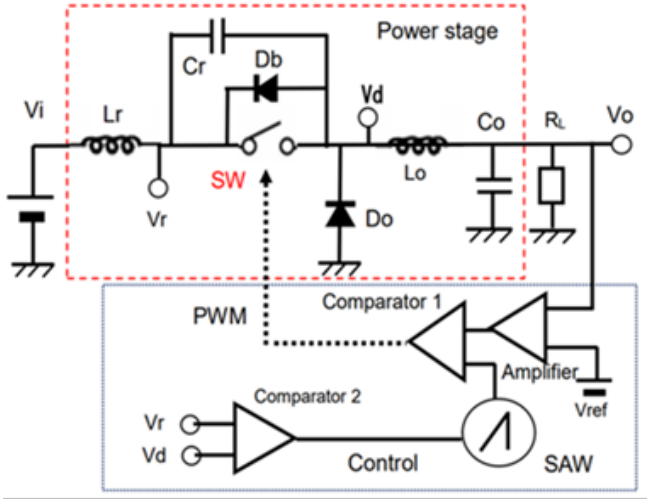


Figure 49. Basic soft-switching converter with half-wave resonance [16] ©JTSS.

7.2. Simulation Results of Half-Wave Voltage Resonant Converter

Figure 50 shows the simulated waveforms of the basic soft-switching converter with half-wave resonance. Table 7 lists the simulation conditions, and its operation is as follows:

State 1: When SW turns off, Lr and Cr start to resonate. As Vr increases, it reaches a peak of approximately 125 V. Then it decreases. During this state, the current through Lo flows also through Do.

State 2: As Vr decreases to the level of Vd, Vb turns ON and it stops the resonance. The output of comparator 2 goes high and it triggers a pulse to the SAW generator. The SAW signal resets, and the PWM signal goes low, turning

the SW on. This results in ZVS, as the voltage across SW is 0 V when it turns on.

State 3: When the resonance stops, Ir flows through Lr in the reverse direction, from the node Vd to the input (Vi) (Figure 46). This reverse current is supplied through Do and it peaks. Then it decreases to 0 A.

State 4: After Ir reaches 0 A, it continues to increase in the forward direction because the voltage across Lr is approximately Vi. Ir increases until it matches the output current (Io), at which point, Do is cut off and Vd rises to Vi. The output voltage (Vo) also increases as the inductor current through Lo increases.

State 5: When Vo reaches Vref, the PWM signal goes low, turning SW off. Then the operation returns to State 1.

The resonance voltage Vr(t) is given by Equations (9), (10). The resonant peak voltage must be larger than Vi (See Equation (11)).

$$Vr(t) = Vi + (Io \cdot Zr) \cdot \sin(\omega t) \tag{9}$$

Here, $$\omega = 1/\sqrt{(Lr \cdot Cr)},\ Zr = \sqrt{(Lr/Cr)} \tag{10}$$

The resonant condition is: $$Vr < 0 \therefore Io \cdot Zr > Vi \tag{11}$$

Features of soft-switching converters are as follows:

1) The resonant peak voltage Vp is very high and it depends on Io and Zr (See Equation (9)).

2) The operation period is unstable due to no usage of clock. To maintain the resonance when Io = 0A, a dummy current Idum is required. It is preferable to keep Idum small for high efficiency, but large Idum simplifies circuit design and reduces peak voltage.

Figure 51 illustrates the simulated waveform of Vo for a current step ΔI of 0.25 A. The steady-state ripple is smaller than 2 mVpp at Io = 0.5 A. The overshoot/undershoot is approximately 15 mV with a current step ΔI of 0.25 A. The settling time is about 0.2 ms. The operating frequency is approximately 380 kHz.

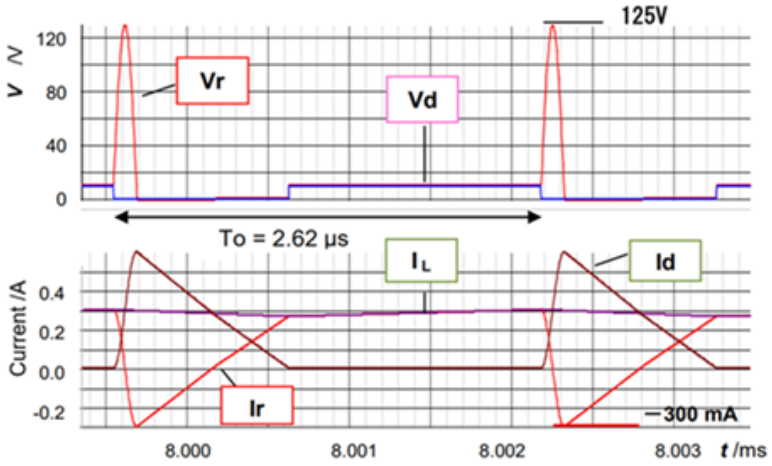


Figure 50. Simulation results of half-wave resonant converter [16] ©JTSS.

Table 7. Simulation conditions of soft-switching converter [16] @JTSS

Parameter	Value
Vi	10.0 V
Vo	5.0 V
Io	0.25 A
Lr	20 µH
Cr	100 pF
Lo	50 µH
Co	220 µF

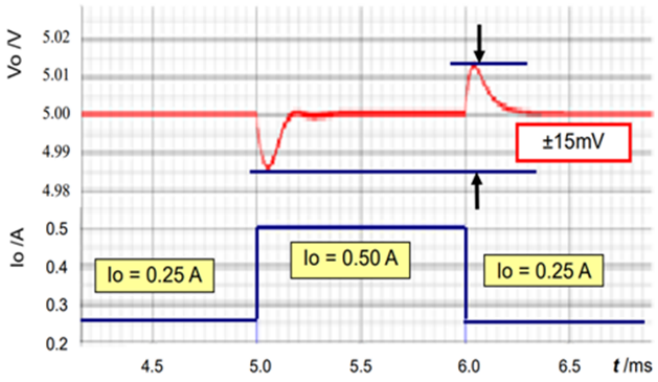


Figure 51. Simulated transient responses of half-wave resonant converter [16] ©JTSS.

7.3. Basic Full-Wave Voltage Resonant Converter

Figure 52 illustrates the soft-switching converter with full-wave voltage resonance. The primary difference from the half-wave voltage resonance converter is the addition of a diode (Dr) in front of SW in series. Figure 53 displays the simulated waveforms of this converter. Notice that the resonant voltage Vr exhibits both positive and negative peaks. The waveform of Vr begins with Vi, passes through both the positive and negative peaks, and ends with the voltage Vd, which is approximately 0 V. The operation of this circuit is similar to that of the half-wave resonant converter. The PWM signal turns high when the resonant voltage Vr returns to around 0 V from the negative resonant voltage (Figure 53). In this circuit, Io is 0.9 A, and the resonant peak voltage reaches 400 V. The conditions are the same as those in Table 7, and the operating frequency is approximately 1.25 MHz.

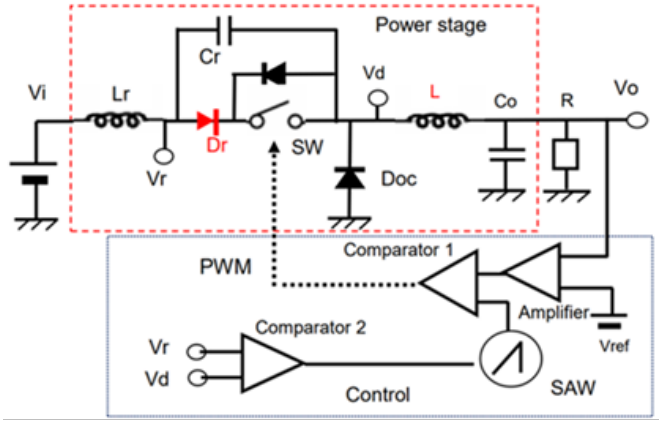


Figure 52. Basic soft-switching converter with full-wave resonance [16] ©JTSS.

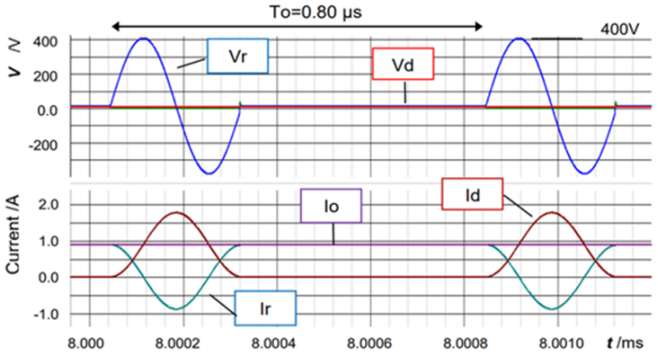


Figure 53. Simulated waveforms of full-wave resonant converter [16] ©JTSS.

7.4. SIDO Soft-switching Converter with Half-wave Voltage

Figure 54 illustrates the SIDO soft-switching converter with half-wave voltage resonance. This converter comprises one power stage, two sub-converters, and a control stage. The control stage includes comparator 1, a selector, comparator 2 (which generates the PWM signal), and comparator 3 (which supplies the trigger pulse to the SAW signal generator). SEL and PWM signals are generated using the exclusive method, whose operation is similar to the SIDO buck-buck converter in Figure 3.

Figure 55 presents the simulated waveforms of this converter with V1 = 5.0 V, V2 = 4.0 V, I1 = 0.50 A and I2 = 0.25 A. Sub-converter 1 is selected when the SEL signal is high. The period of each cycle varies, and the peak level of the inductor current IL fluctuates between 750 mA and 830 mA, averaging around 700 mA. The peak level of Vr remains nearly constant at 55 V. The operation period ranges from 3.5 µs to 7.0 µs. Figure 56 displays the simulated output voltage ripples, which are smaller than 5 mVpp for I1 = 0.50 A, I2 = 0.25 A. The maximum ripple is approximately 10 mVpp for I1 = 0.75 A, I2 = 0.25 A. The over/under-shoots are approximately 5 mV for a current step ΔIo = 0.25 A.

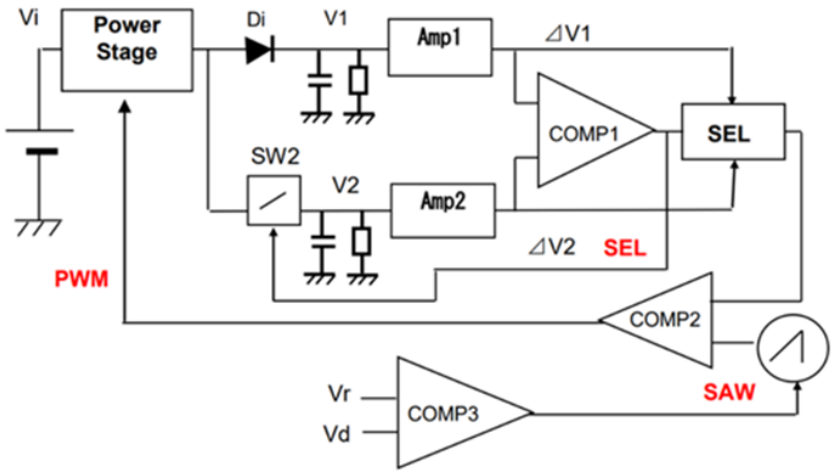


Figure 54. SIDO soft-switching converter circuit with half-wave voltage [16] ©JTSS.

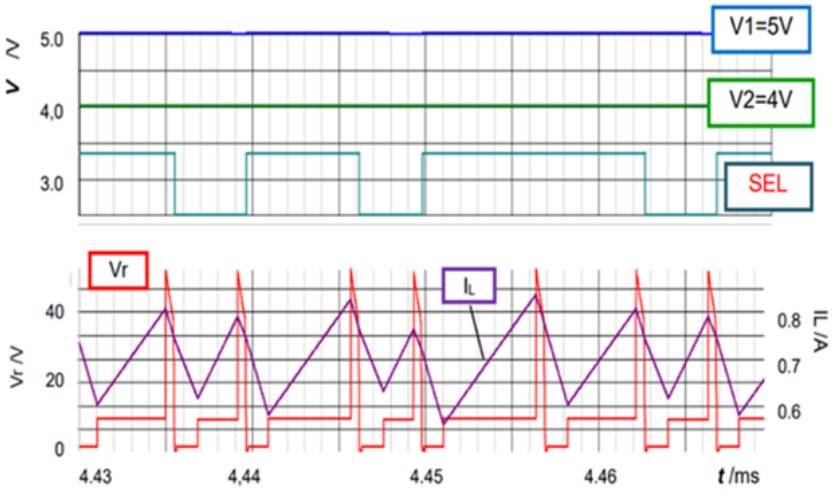


Figure 55. Simulated waveforms of Figure 54 [16] ©JTSS.

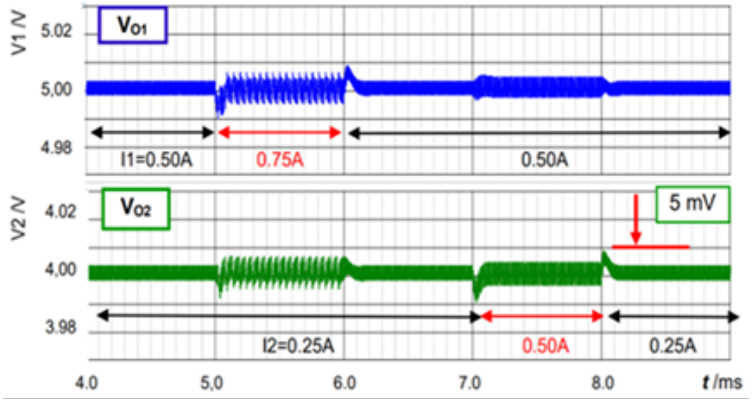


Figure 56. Simulated transient responses of Figure 54 [16] ©JTSS.

8. Single Ended Primary Inductor Converter (SEPIC)

8.1. Basic Buck-Boost SEPIC

In this section, we focus on SEPIC converters and their modified configurations, then expand them to multi-output SEPICs using our exclusive control method. The typical chopper-type buck-boost converter is illustrated in Figure 57, and the output voltage is given by Equation (12) with a "negative polarity" output. (This configuration was previously introduced in Section 3, Figure 4.)

$$Vo = -D/(1 - D) \cdot Vi \tag{12}$$

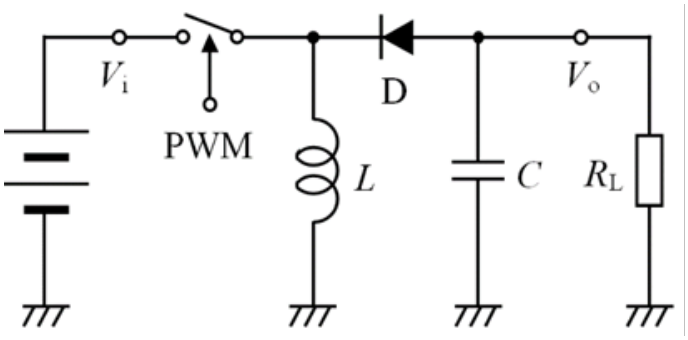


Figure 57. Chopper-type buck-boost converter.

8.1.1. Buck-Boost SEPIC

Configuration: The basic SEPIC converter in Figure 58 is a buck-boost converter with "positive polarity" output. It requires an additional inductor L1 and a capacitor C1 to achieve the positive polarity output. The main power switch and the primary inductor Lin are positioned similarly to the chopper-type boost converter in Figure 4.

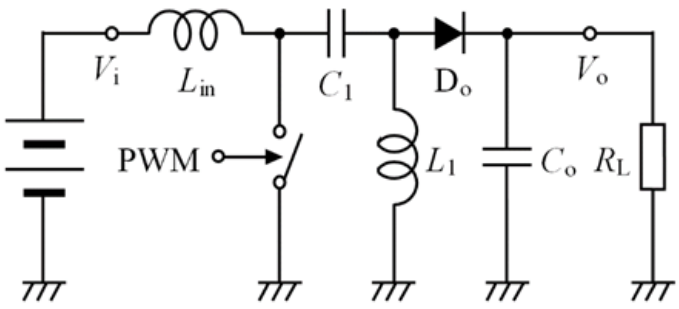


Figure 58. Configuration of buck-boost SEPIC.

Operation: SW is controlled by a PWM pulse, toggling between on and off states. When SW is on, the energy in the inductor Lin increases with the input current, as indicated by the green line in Figure 59. Concurrently, the charge of capacitor C1 decreases through inductor L1, transferring energy from C1 to L1. The voltage across L1 is approximately −Vi (<0 V), and the diode Do remains off. When SW turns off, the energy from both inductors flows to the bulk capacitor Co and the load resistor RL, as indicated by the red line. The voltage at the edge of L1 is nearly Vo. In this scenario, the output polarity is "positive," and the output voltage Vo is given by Equation (13):

$$Vo = +D/(1 - D) \cdot Vi \tag{13}$$

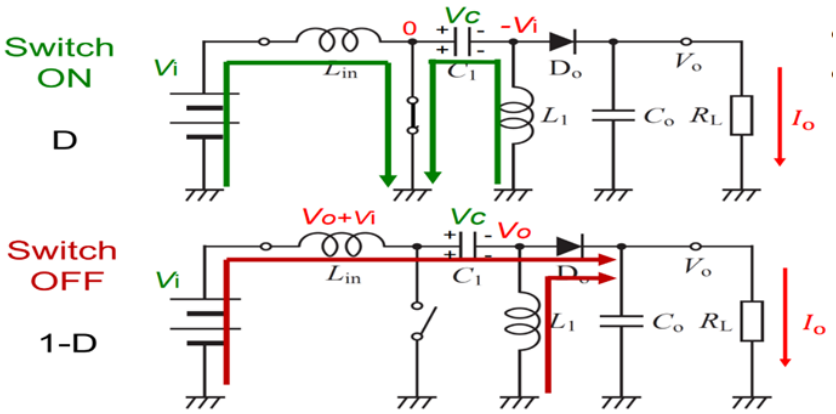


Figure 59. Operation of buck-boost SEPIC.

8.1.2. High Boost SEPIC

Configuration: The converter in Figure 60 produces a higher output voltage for a given duty ratio (D) due to the additional diode (Db) and capacitor (Cb), compared to the buck-boost SEPIC in Figure 58.

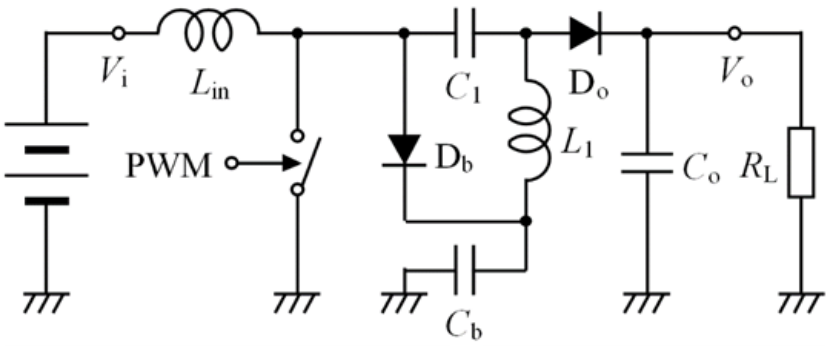


Figure 60. Configuration of high boost SEPIC [14] ©IEEE.

Operation: The switch (SW) and the main inductor (Lin) are controlled in the same manner as in the buck-boost SEPIC. When SW is on, the currents through both inductors are depicted by the green lines in Figure 61. The voltage (Vc) across capacitor C1 increases with the current from L1 and the additional capacitor Cb. The polarity of Vc is reversed compared to the polarity of Vc in the buck-boost SEPIC (Figure 59). When SW turns off, the currents from both inductors flow to the bulk capacitor (Co) and the load resistor (RL), and Cb is charged through the additional diode (Db).

However, the high boost SEPIC does not function as a buck converter. The output voltage (Vo) is higher than the input voltage (Vi) as shown in Equation (14):

$$Vo = +(1 + D)/(1 - D) \cdot Vi \tag{14}$$

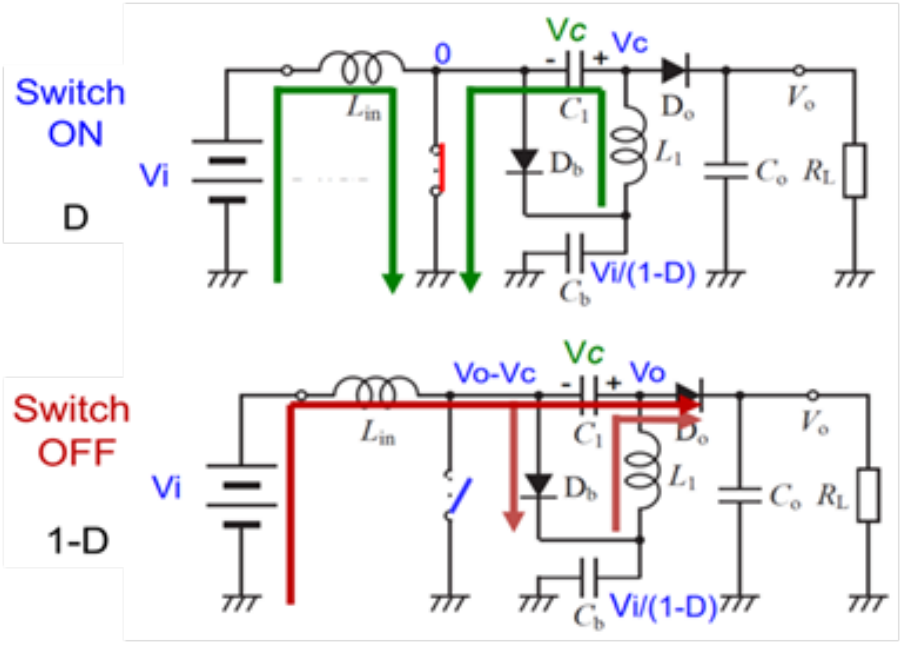


Figure 61. Operation of high-boost SEPIC [14] ©IEEE.

8.1.3. Multiplied Boost SEPIC

This converter incorporates additional LC and D ladder circuits (Figure 62). Each ladder circuit boosts the voltage, resulting in a very high final output voltage (Vo) as shown in Equation (15):

$$Vo = +(1 + 3D)/(1 - D) \cdot Vi \tag{15}$$

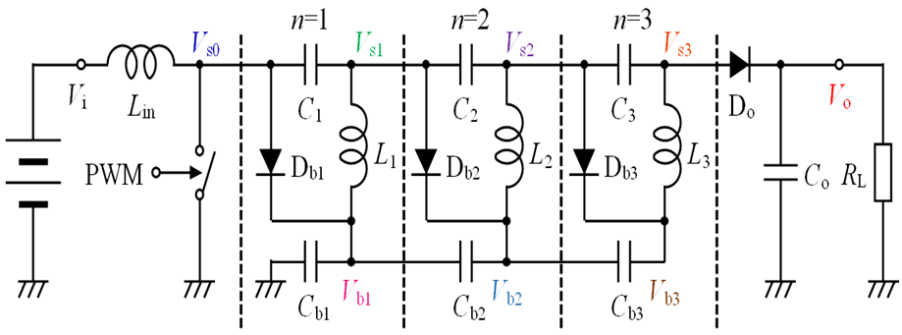


Figure 62. Configuration of multiplied boost SEPIC [14] ©IEEE.

8.2. Dual-Output Buck Boost SEPIC

8.2.1. Configuration and Operation

We review here the dual-output buck-boost SEPIC based on the circuit in Figure 58. Its power stage is illustrated in Figure 63, where two inductors (Lin, L1), one capacitor (C1), and one switch (SW1) are shared. This converter functions as both a boost converter (Vo1) and a buck converter (Vo2), meaning Vo1 is higher than Vi and Vo2 is smaller than Vi (Vo1 > Vi > Vo2 > 0).

In this configuration, a diode (DO2) is required in front of the switch (SW2) in the buck converter. This is because the switch (SW2) is an NMOS transistor, which includes a body diode across it (Figure 63). Without DO2, this body diode would turn ON when the main switch (SW1) is ON, due to the voltage (Vs2) across L1 becoming negative (−Vi) (Figure 59). The control stage is the same as the previous SIDO buck-buck converter (Figure 8).

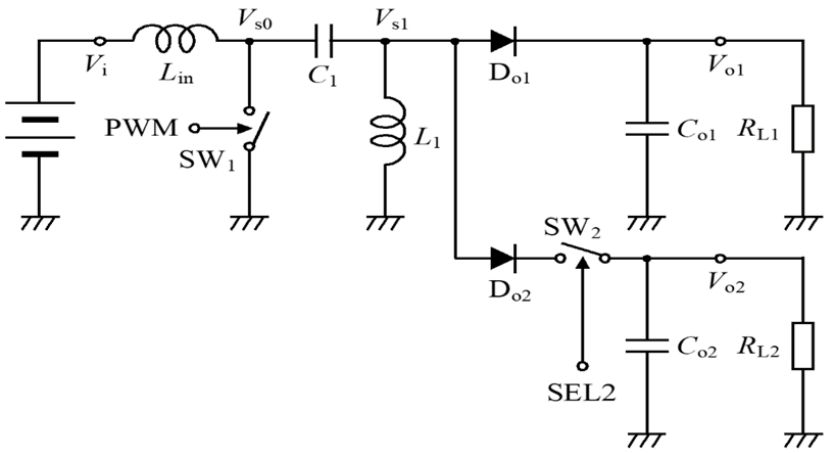


Figure 63. Configuration of power stage of dual-output buck boost SEPIC [14] ©IEEE.

8.2.2. Simulation Results

Figure 64 shows the simulated waveforms of the dual-output buck-boost SEPIC depicted in Figure 63, while Figure 65 illustrates its transient responses. The simulation conditions are in Table 8. These input-output conditions assume Li-ion batteries as the power source, driving wearable devices and portable equipment. In the dual-output configuration for step-up and step-down power supplies, the same power stage operates over a wide range of boost and buck ratios.

From Figure 64, we observe that for output currents Io1 = 10 mA, Io2 = 50 mA, and he steady-state ripples are ΔVo1 = 2.5 mV, ΔVo2 = 0.8 mV, with an efficiency of 80.8%. Additionally, Figure 65 reveals the following:

(i) Output current variations on the Vo1 side: for a output current change of ΔIo1 = 10 mA, the overshoot is ΔVos1 = 13.5 mV, and for the Vo2 side, it is ΔVos2 = 1.2 mV.

(ii) Output current variations on the Vo2 side: for a output current change of ΔIo2 = 50 mA, the overshoot is ΔVos1 = 22 mV, and for the Vo2 side, it is ΔVos2 = 2.4 mV.

Table 8. Simulation conditions for dual-output buck boost SEPIC.

Parameter	Value	Parameter	Value	Parameter	Value
Vi	4.0 V	fck	500 kHz	Ci	10 µF
Vo1	12.0 V	Lin	200 µH	Ci ESR	1 mΩ
Vo2	1.8 V	Lin ESR	20 mΩ	Co1	100 µF
Io1	10 mA → 20 mA	L1	220 µH	Co1 ESR	1 mΩ
Io2	50 mA → 100 mA	L1 ESR	20 mΩ	Co2	470 µF
				Co2 ESR	1 mΩ

8.3. Dual-Output Mode-Change High Boost SEPIC

When the buck-boost SEPIC in Figure 58 is used in the power stage, it allows for both step-up and step-down operations. However, the duty ratio increases significantly when a high boost ratio is required. Conversely, using the high-boost SEPIC in Figure 60 can mitigate the increase in duty ratio during high-boost operation, but it cannot perform step-down operations.

By switching the power stage between the buck-boost SEPIC and the high-boost SEPIC, we explored a configuration where one of the dual outputs is a step-up output (Vo1) suitable for high boost, and the other is a step-up/down output (Vo2).

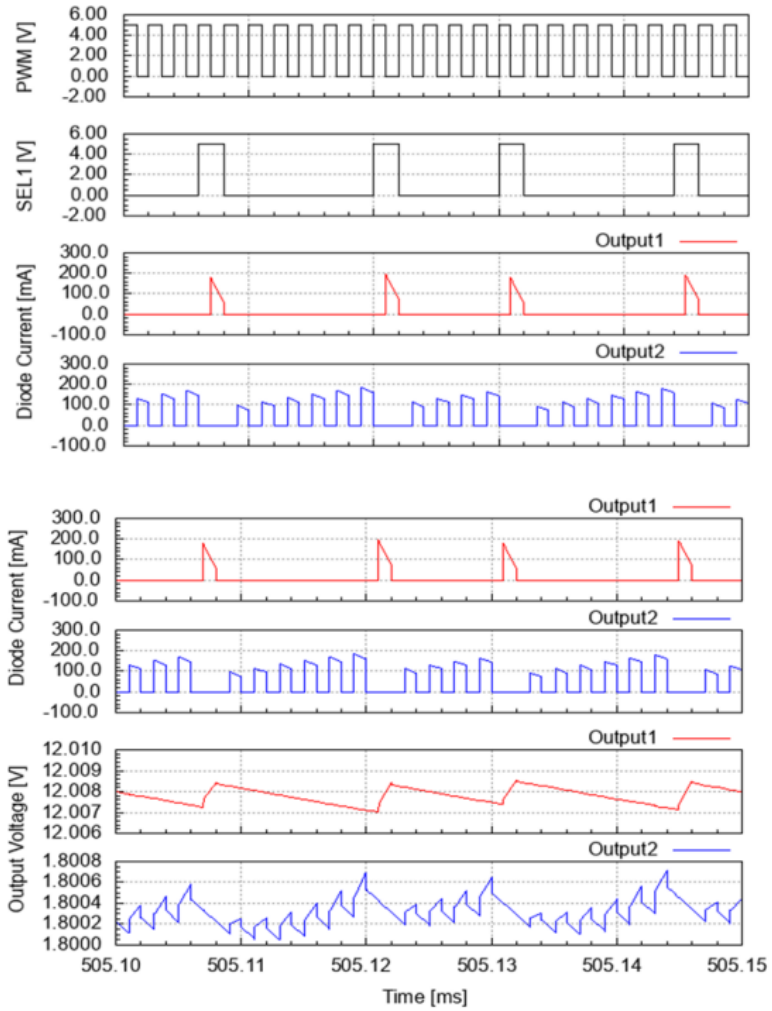


Figure 64. Simulation results of dual-output buck boost SEPIC [14] ©IEEE.

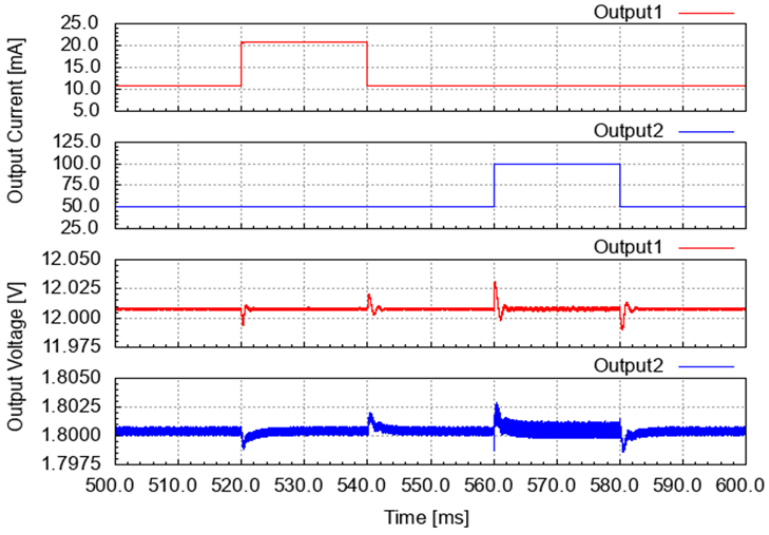


Figure 65. Transient response of dual-output buck boost SEPIC [14] ©IEEE.

8.3.1. Configuration and Operation

Figure 66 illustrates the configuration of the dual-output mode change high boost SEPIC. A switch (SWb) is placed in series with a diode (Db), and a switch (SWs) is placed in parallel with a capacitor (Cb). These switches are driven by the output selection signals (SEL1, SEL2). During step-up operation, the high-boost SEPIC configuration is used, while during step-down operation, the buck-boost SEPIC configuration is employed. For the buck-boost SEPIC configuration, SWb is turned off and SWs is turned on. Conversely, for the high-boost SEPIC configuration, SWb is turned on and SWs is turned off.

During the initial control cycle of the configuration switch, the voltage across Cb and the current through L1 are in a transient state, resulting in a large spike-like current flowing into the output capacitors (Co2) and generating noise in the output voltage (Co2). To address this, an output selection switch (SWo2) is provided for the output (Vo2), which turns on one control cycle after the output selection switch is toggled, reducing the output voltage ripple. Similarly, an output selection switch (SWo1) is provided for the output (Vo1) to handle noise-induced voltage spikes. Figure 67 illustrates a control circuit with the added output control. The error amplifiers, PWM pulses (PWM1, PWM2), and selection signals (SEL1, SEL2) are generated in the same configuration as in Figure 8 of Section 2.

Detection of the configuration switch change is performed during the first control cycle using the exclusive logical OR of the selection signal and its one-control-cycle-delayed version. By forcibly turning off the selection signals (SEL1, SEL2) only during configuration changes, the drive signals (OEN1, OEN2) for the output selection switches are generated.

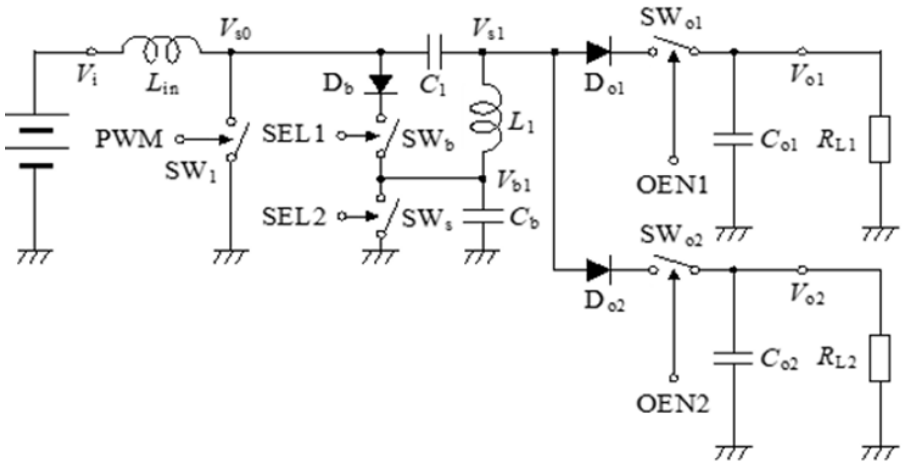


Figure 66. Power stage configuration of dual-output mode-change high boost SEPIC [14] ©IEEE.

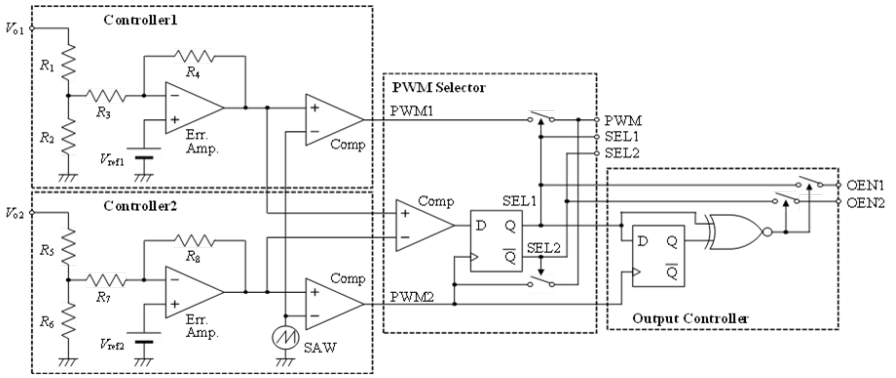


Figure 67. Control stage of dual-output mode-change high boost SEPIC [14] ©IEEE.

8.3.2. Simulation Results

Figure 68 illustrates the simulated waveforms of the dual-output mode-change SEPIC in Figure 66. Figure 69 shows its transient response characteristics. The input-output conditions and various circuit conditions are listed in Table 9.

In the dual-output mode-change power supply, the same power stage operates over a wide range of step-up and step-down ratios. For each output with currents Io1 = 10 mA and Io2 = 50 mA, the steady-state ripples are ΔVo1 = 2.7 mV and ΔVo2 = 1.7 mV, with an efficiency of 79.6%. Regarding the overshoot voltage for an output current change ΔIo1 = 10 mA on the output Vo1 side, they are ΔVos1 = 13.8 mV and ΔVos2 = 2.5 mV. Similarly, for an output current change ΔIo2 = 50 mA on the output Vo2 side, the overshoot are ΔVos1 = 13 mV and ΔVos2 = 1.5 mV.

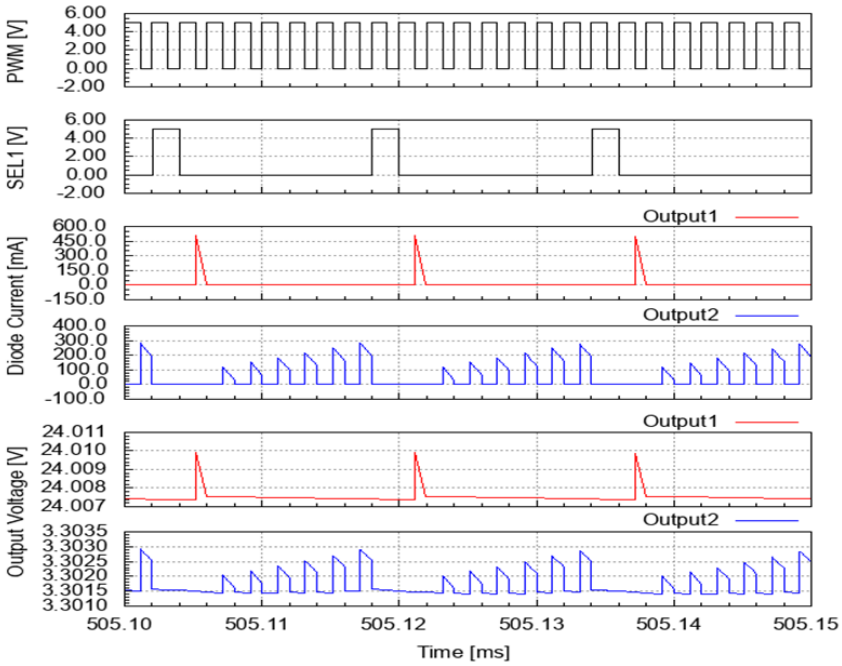


Figure 68. Simulation results of dual-output mode-change high boost SEPIC [14] ©IEEE.

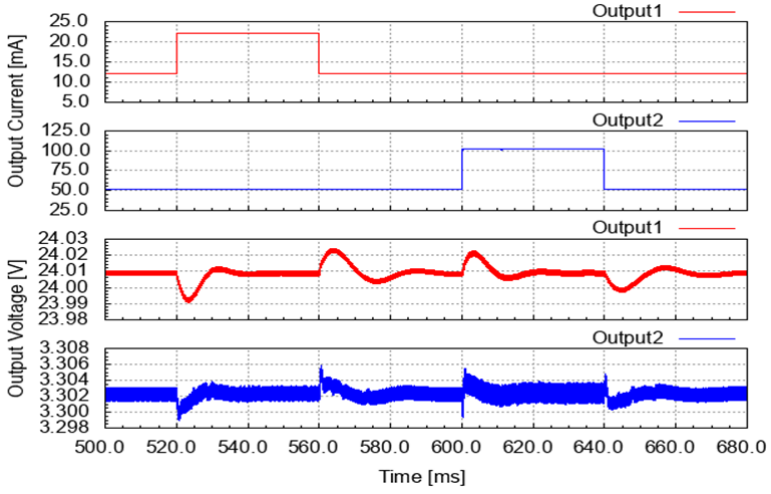


Figure 69. Transient responses of dual-output mode-change high boost SEPIC [14] ©IEEE.

Table 9. Simulation conditions for dual-output mode-change high boost SEPIC

Parameter	Value	Parameter	Value	Parameter	Value
Vi	4.0 V	fick	500 kHz	Ci	5 µF
$Vo1$	24.0 V	Lin	220 µH	Ci ESR	5 mΩ
$Vo2$	3.3 V	Lin ESR	20 mΩ	$Co1$	1 mF
$Io1$	10 mA → 20 mA	$L1$	220 µH	$Co1$ ESR	5 mΩ
$Io2$	50 mA → 100 mA	$L1$ ESR	20 mΩ	$Co2$	2 mF
				Co2 ESR	5 mΩ

9. Multi-Output Converter with Four Outputs

9.1. Single-Inductor Multi-Output (SIMO) Buck Converter

9.1.1. Configuration and Operation

Figure 70 illustrates the SIMO buck converter, which includes the power stage and four plug-in sub-converters. Each sub-converter is equipped with a standard output capacitor, an operational amplifier, a reference voltage source (Vr), and additional components such as an input select diode, a select switch, a PWM pulse generator (comparator 1), a select signal generator (comparator 2), and an FF. An error voltage (ΔVo) and a PWM pulse are generated within each sun-converter. The main switch (SW) is controlled by the PWMo pulse, which is the aggregate of the individual PWM pulses.

Figure 71 depicts the circuit that generates a common maximum voltage (Vcom), based on each ΔVo. This voltage (Vcom) is provided to each sub-converter for the select signal generation, which controls the switch in the sub-converter. The wired OR circuit is employed to decide which sub-converter will be served in the next period (Figure 71).

This circuit provides the largest error voltage (Vdv) to each comparator. For instance, if ΔV1 is the largest among all the voltages (ΔV1 to ΔV4), the voltage (Vdv) at the OR output node will be ΔV1 - Vsel, where Vsel is the voltage across the selected diode. In this scenario, R1 is much larger than R2, setting the voltage Vcom smaller than Vsel. Consequently, SEL1 goes high, and the switch in the sub-converter 1 turns ON.

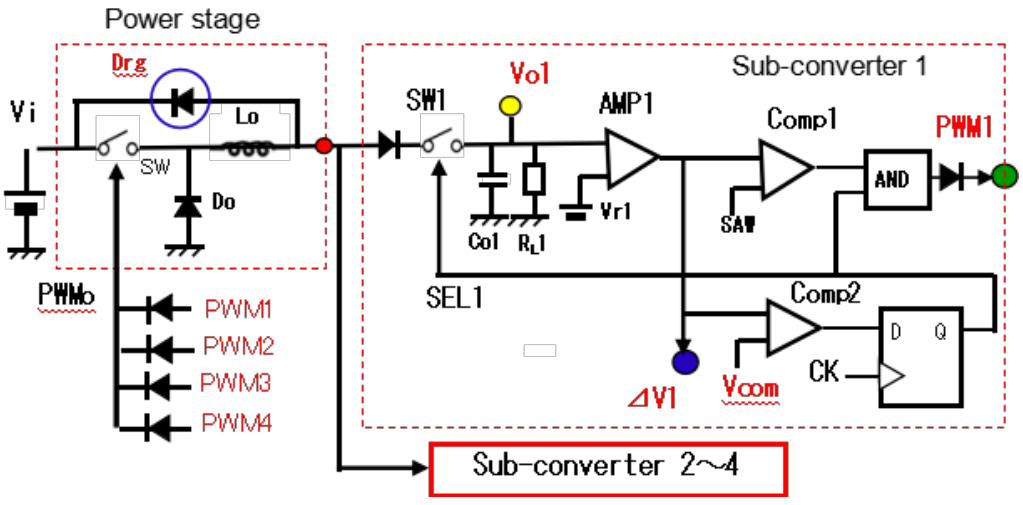


Figure 70. SIMO buck converter with four outputs [16] ©JTSS.

9.1.2. Simulation Verification

Figure 72 illustrates the simulated waveforms of the SIMO converter with four output voltages, V1 to V4. Each sub-converter has a static current of 0.5A, and the output current change ΔIo for I1 or I4 is 0.5A. Table 10 shows its simulation conditions. There, only one select signal is active (Figure 73). When the output voltage of each sub-converter exceeds its corresponding reference voltage, all the select signals (SEL1 to SEL4) become low, and no

switch in any sub-converter is selected. This scenario is depicted in Figure 73; no active SEL signal duration is marked with a star. There, the regenerated inductor current Ir flows into the input voltage source through the diode (Drg).

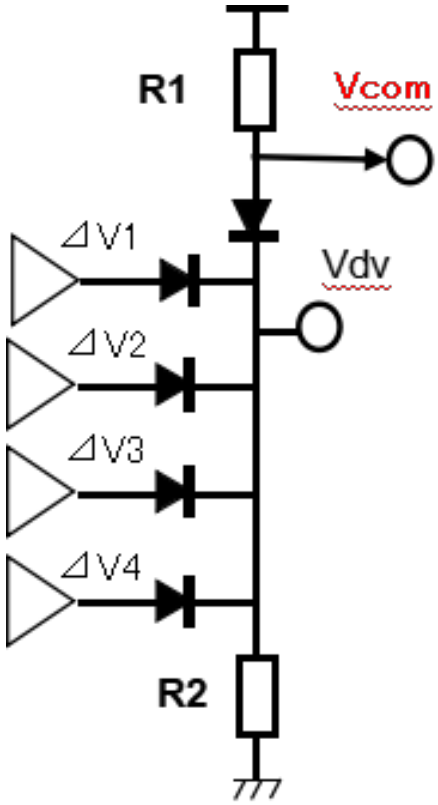


Figure 71. Control stage [16] ©JTSS.

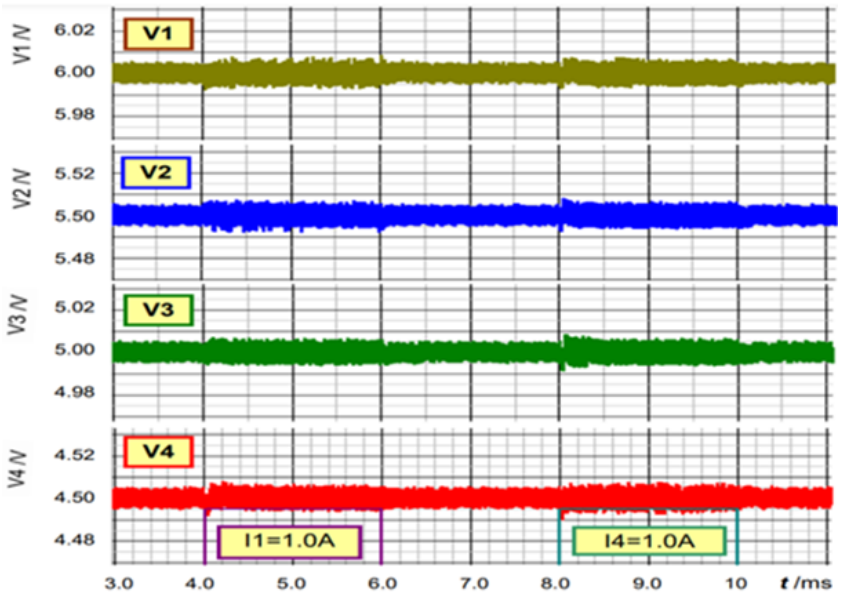


Figure 72. Simulated waveforms of SIMO buck converter with four outputs [16] ©JTSS.

Table 10. Simulation conditions of SIMO buck converter.

Parameter	Value
Vin	10.0 V
$V1$	6.0 V
$V2$	5.5 V
$V3$	5.0 V
$V4$	4.5 V
Io	0.5 A (for each)
L	0.2 µH
C	470 µF (for each)
Fck	500 kHz

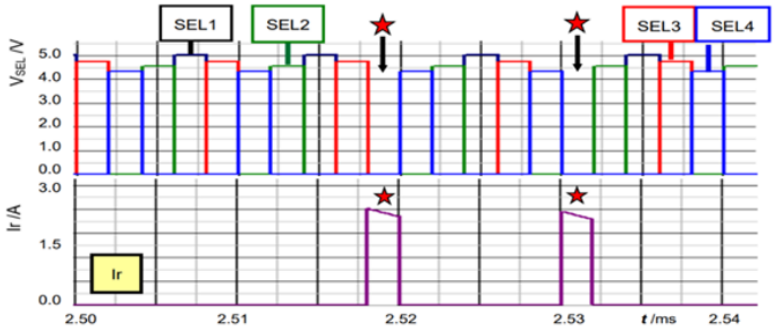


Figure 73. Simulation results of SIMO buck converter with four outputs [16] ©JTSS.

9.2. Multi-Output Multiplied Boost SEPIC

9.2.1. Configuration and Operation

We review a four-output multiplied boost SEPIC based on the circuit in Figure 62. Its power stage is illustrated in Figure 74, while the control stage is in Figure 75. The relationship between each output voltage is set as Vo1 > Vo2 > Vo3 > Vo4. We configured the power stage of the multiplied-boost output SEPIC to obtain four voltages by connecting each output diode to nodes Vs3, Vs2, and Vs1. Unlike the dual-output configuration, when connecting output diodes to different nodes, selection switches are provided for all outputs.

It is also possible to achieve a four-output configuration by connecting output diodes to nodes Vb1, Vb2 and Vb3, instead of Vs1, Vs2, and Vb3. However, we found that doing so increases the output voltage ripple. In the multiplied boost SEPIC, the output voltage ripple is primarily dominated by the pulse current when the output diode Do conducts during switch off-time. When extracting output current from nodes Vb1, Vb2, and Vb3, a spike-like current flows through the output diode Do immediately after the selection signal switches during PWM rise time. This spike current is significantly larger compared to the output diode current during switch off-time, and it contributes to increased output voltage ripple by flowing through the equivalent series resistance (ESR) of output capacitor Co. Then our original configuration in Figure 75 is better.

In the control stage, we extend the dual-output configuration to selectively control the most prioritized output and its corresponding PWM pulses. This prioritized exclusive control circuit is shown in Figure 75. The error amplification voltage of the operational amplifier is denoted as Verrn. These maximum voltages, Verrm, are generated using a diode OR circuit. Each Verrn is compared against Verrm by a comparator. When Verrn exceeds Verrm (i.e., Verrn becomes the largest error amplification voltage), the comparator output goes to a high level, indicating the need for current supply. If multiple comparator outputs are high, the output with the highest set voltage takes priority.

Specifically, the priority order is SEL1 > SEL2 > SEL3 > SEL4, forcibly turning off the smaller-voltage output. The SEL signal determines which PWM pulses from each control circuit drive the main switch.

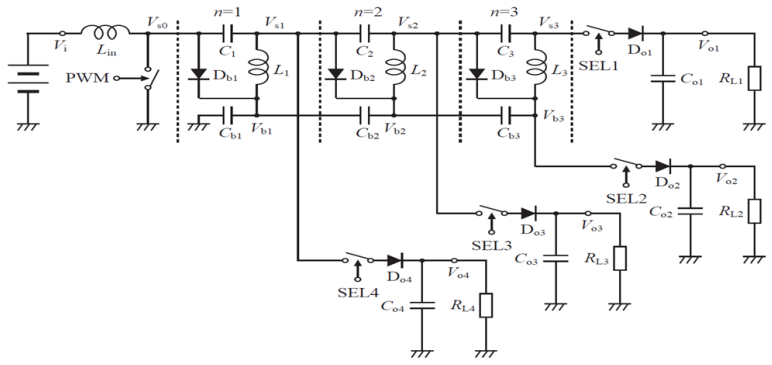


Figure 74. Configuration of four-output multiplied boost SEPIC [14] ©IEEE.

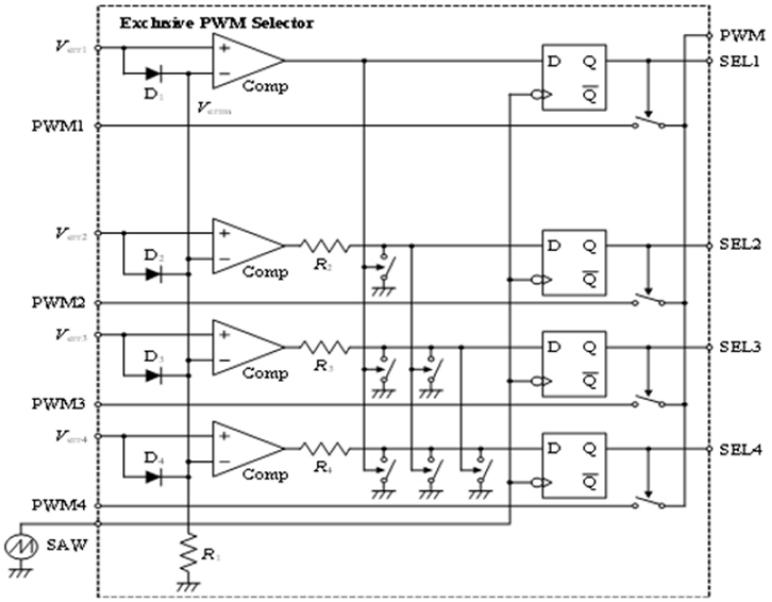


Figure 75. Control stage of four-output multiplied boost SEPIC [14] ©IEEE.

9.2.2. Simulation Results

Figure 76 shows the simulated waveforms of the multi-output multiplied high boost SEPIC. The input-output conditions are shown in Table 11. The circuit conditions are based on the values in Table 9. Each SEL signal generates pulses exclusively, and the pulse current during selection causes pulse-like ripple in the output voltage. Note that the output ripple (ΔVo) is smaller than 1.0 V.

Table 11. Simulation conditions of multi-output multiplied boost SEPIC

Parameter	Value	Parameter	Value	Parameter	Value
Vi	12 V	$Io3$	100 mA	$C1$, $C2$, $C3$	5 µF
$Vo1$	160 V	$Io4$	100 mA	$C1$, $C2$, $C3$ ESR	5 mΩ
$Vo2$	120 V	fck	500 kHz	$Cb1$, $Cb2$, $Cb3$	1 mF
$Vo3$	80 V	Lin	22 µH	$Cb1$, $Cb2$, $Cb3$ ESR	5 mΩ
$Vo4$	40 V	Lin ESR	20 mΩ	$Co1$, $Co2$, $Co3$	1 mF
$Io1$	150 mA	$L1$, $L2$, $L3$	220 µH	$Co1$, $Co2$, $Co3$ ESR	5 mΩ
$Io2$	150 mA	$L1$, $L2$, $L3$ ESR	20 mΩ		

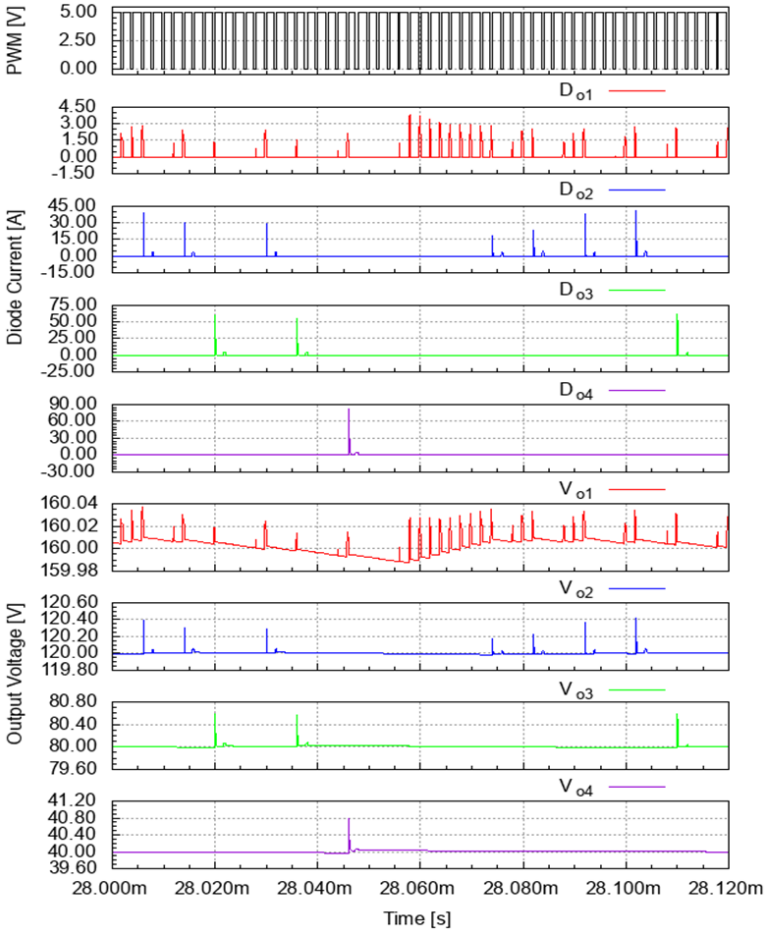


Figure 76. Simulation results of multi-output multiplied boost SEPIC [14] ©IEEE.

10. Conclusions

This paper reviews technologies of SIDO and SIMO DC-DC switching converters with the PWM, hysteretic, ZVS-PWM, soft-switching controls and SEPICs using our proposed exclusive control method. These converters can decrease the inductor count and minimize the converter size. These converters are composed of a power stage with a single inductor and two sub-converters. The exclusive control ensures that the power stage supplies power to the sub-converter with the larger error voltage throughout the entire period.

In the SIDO converter utilizing hysteretic control, the RC network that generates the triangular signal is connected to the output of sub-converter 1, as the voltage at the tail edge of the inductor varies with the SEL signal. In the SIDO converter using the ZVS-PWM control, the reverse current that charges the resonant capacitor $C\ r$ is consistently provided by sub-converter 2. The SIDO converter with the soft-switching control has a problem that the resonant peak voltage becomes high for the large output current. In the dual-output SEPIC, the tail voltage of the coupling capacitor C1 becomes negative voltage -Vi so that the series diode Do2 is needed before the switch SW2 due to the body diode of the NMOS switch.

In the SIMO converter with four outputs, the wired OR circuit is used to determine which sub-converter will be regulated in the next period. When no sub-converter is selected, the regenerated inductor current flows into the input voltage source through the free-wheel diode connected to the tail edge of the inductor.

The features of the exclusive control for the SIMO DC-DC converter are as follows:

(1) No current sensor is needed.

(2) Output voltage ripple can be minimized because the sub-converter with the highest priority, typically the one with the greatest output deviation, is served first.

(3) A fast transient response can be achieved because the sub-converter with the highest priority, typically the

one with the greatest output deviation, is taken care of first.

(4) The next step is to address cross-regulation and efficiency considerations in case of the exclusive control usage.

The SIDO converters reviewed in this paper should be used appropriately depending on the application. The duty ratio of the select signal SEL of SIDO converter is suitable for the current balance of each sub-converter. In recent years, when the output current difference between SIDO converters is significantly large, current-mode controlled converters have become mainstream; it is expected that SIDO converters using this method will prevail in the future. Another significant problem in the switching converter is EMI noise, which is unnecessary radiation or conducted noise. For addressing this problem, a simple ZVS-PWM controlled converter or a half-wave/full-wave type resonant soft-switching converter is highly effective. However, the remained small radiation noise is affective to the radio receivers. One of the solutions is a noise spectrum spreading technique. Also, for a precise evaluation of the proposed circuit implementation, an electromagnetic field analysis including layout and interconnection of components would be helpful.

Author Contributions

Conceptualization, Y.K. and H.K.; methodology, Y.K.; data curation, Y.K.; writing—original draft preparation, Y.K.; writing—review and editing, H.K.; funding acquisition, H.K. All authors have read and agreed to the published version of the manuscript.

Funding

This work was supported by Asahi Kasei Power Devices Corp.

Institutional Review Board Statement

Not applicable.

Informed Consent Statement

Not applicable.

Data Availability Statement

All data are shown in the authors' published papers cited in this paper.

Acknowledgments

All members and research collaborators in our laboratory who contributed to the research described in this paper are acknowledged.

Conflicts of Interest

The authors declare no conflict of interest.

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