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*Review*

# Overview and Recent Report of Integrated Filter Design Employing Frequency Dependent Negative Resistor (FDNR)

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**Abstract:** Filters are essential circuits for various signal processing circuits. One of the main methods of filter integration is to design an LC filter first as a prototype filter, and then simulate the function of the inductor with active components. Considering that the accuracy of elements implemented on a semiconductor chip is significantly lower than that of individual elements, this method, which uses a resistive doubly terminated LC ladder filter with low element sensitivity as the prototype, has been widely adopted. The Bruton Transformation is known as one of the methods to integrate the LC filter. The method avoids the use of inductor elements, which make integration difficult, and requires a component called a Frequency Dependent Negative Resistor (FDNR) . An FDNR is a negative resistance whose impedance is inversely proportional to the square of the frequency. Because the FDNR does not exist as a passive element, it is realized using an active block such as an operational amplifier. This paper provides an overview of the Bruton Transformation and the FDNR. The first half of this paper briefly describes the Bruton transformation and reviews the FDNRs proposed to date since the Bruton transformation was first presented. The second half of the paper presents the latest examples of filter integration methods using FDNR proposed by the authors.

**Keywords:** Analog Integrated Circuits; LC Filters; Bruton Transformation; FDNR (Frequency Dependent Negative Resistor)

## 1. Introduction

Anti-aliasing low-pass filters are essential circuits for digital signal processing in various electronic devices. In addition, filters have a wide variety of uses, such as high-pass filters that cut DC components and band-pass filters that pass only necessary bands. Looking back at the history, it seems that the origin of the filter is an invention presented in 1915 by G. Campbell in the U.S. and K. Wagner in Germany. They independently proposed the basic concept of filters at about the same time. Subsequently, with the advent of the reactance theorem, image parameter theory, and positive real function theory, design methods for LC filters had been developed in which the reactance function is formed by inductors and capacitors, which are concentrated constant elements. Starting with the invention of the transistor by W. Shockley, J. Bardeen, and W. Brattain in 1948, and the invention of integrated circuits by the J. Kilby patent in 1958 and the R. Noyce patent in 1959, the integration of various electronic circuits was pursued. In the integration of LC filters, it is difficult to implement an inductor with a wound structure to form a magnetic flux inside on a chip. Furthermore, if the cutoff frequency is below the megahertz range, the size of the inductor becomes large. Therefore, researchers at that time investigated methods to realize the function of inductance using semiconductor elements.

Since then, the filter integration techniques that have been used up to the present can be roughly classified into two approaches. One is to factorize the denominator polynomial of the higher-order transfer function derived from the specification into second-order and first-order (odd-order only) sections. The modules of the sections consist of a combination of resistors, capacitors, and active blocks such as operational amplifiers, and are cascaded to construct a desired filter. While this method is easy to design, a block with a high $Q$ value is required, which limits the dynamic range and increases the spread of resistance and capacitance values. The other method is to design an LC filter first as a prototype filter, and then simulate the function of the inductor with active components. This type of filter is called an LC simulation type active filter. Considering that the accuracy of elements implemented on a semiconductor chip is significantly lower than that of individual elements, this method, which uses a resistive doubly terminated LC ladder filter with low element sensitivity as the prototype, has been widely adopted [1].

Two methods are known to realize LC simulation type active filters. The first method is to combine an active block called a gyrator and a capacitor to realize the same impedance as an inductor. This method is called the direct method because each element of the prototype filter and the integrated filter have a one-to-one correspondence. In the first proposed circuit [2], an operational amplifier was used as an active component to compose the gyrator, but gyrators using Operational Transconductance Amplifiers (OTAs) became the mainstream later. In addition, it was found that the gyrator proposed by Riordan can realize various impedance elements other than inductors [2], and it became known as a Generalized Impedance Converter (GIC). The second method is called leapfrog simulation. This method represents each node voltage and current flowing through the elements in the prototype LC filter as a signal flow graph, and simulates the function of the filter with analog operation circuits that performs addition, subtraction, integration, etc. of the signal voltage and the signal current [3]. This method is based on a different principle from the direct method and is called the indirect method. In this method, an operational amplifier was initially used as an active component, and an analog operation circuit was constructed by combining resistors and capacitors. Later, OTAs came to be widely used in place of operational amplifiers. The reason for this is that a differential input OTA can easily add and subtract signals as currents, and an integrator can be easily constructed with only one OTA and one capacitor.

This paper describes the Bruton Transformation which is known as one of the direct methods, and the element called Frequency Dependent Negative Resistor (FDNR) generated by the transformation [4]. Even if all the impedance elements composing the filter are multiplied by the same coefficient, the transfer characteristics do not change. The Bruton Transformation focuses on this point and multiplies the impedance of all elements composing the filter by a coefficient $1/s$ using the Laplace operator $s$. By converting the impedance $sL$ of the inductor into a resistive element with a value of $L$, it is possible to achieve integration without the need for inductors.

This paper is structured as follows. Section 2 briefly explains the Bruton Transformation. Section 3 looks back on the FDNRs proposed since the proposal of the Breton Transformation up to the present day. Section 4 presents the latest examples of filter integration methods using FDNR. Section 5 provides the conclusion.

## 2. Bruton Transformation

The Bruton Transformation method multiplies the impedance of each passive element in the filter by a factor $1/s$ using the Laplace operator $s$ [4]. Multiplying the impedance of each inductor, resistor, and capacitor by a factor $1/s$ yields the following equations.

$$sL\frac{1}{s} = L \tag{1}$$

$$\frac{1}{sC}\frac{1}{s} = \frac{1}{s^2C} \tag{2}$$

$$R\frac{1}{s} = \frac{R}{s} \tag{3}$$

As shown in **Figure 1**, an inductor is converted to a resistor, a resistor to a capacitor, and a capacitor to a $D$ element. Setting $s = j\omega$, the impedance $Z_D$ of the $D$ element is expressed as

$$Z_D = -\frac{1}{\omega^2 D} \tag{4}$$

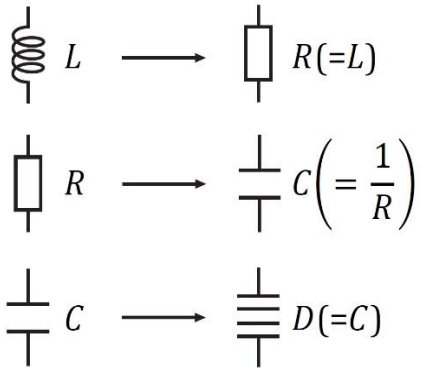


**Figure 1**. Bruton Transformation.

This is called Frequency Dependent Negative Resistor (FDNR) because it is a negative impedance that depends on $\omega^2$. Since such an element does not exist as a passive element, it is realized by active components.

In the work by Bruton [4], a realization method of FDNR using GIC was proposed along with the concept of Bruton Transformation. The circuit configuration of the GIC is illustrated in **Figure 2**. The combined impedance of this circuit is expressed as

$$Z_i = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \tag{5}$$

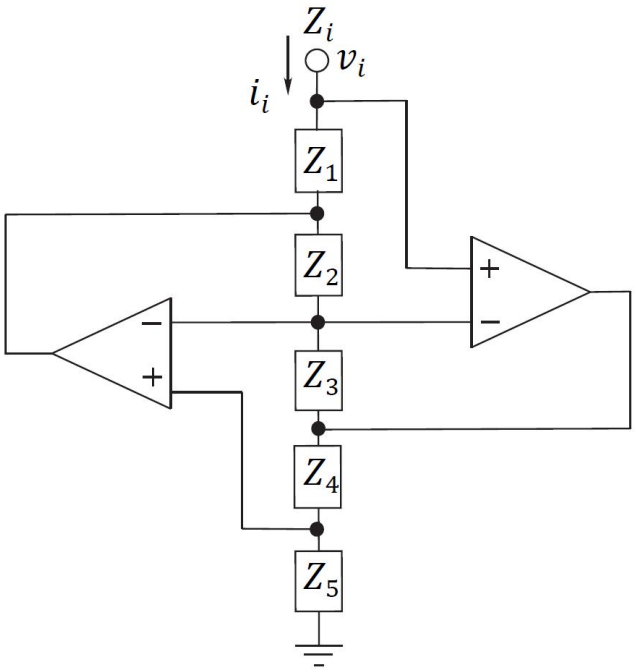


**Figure 2**. Circuit Configuration of GIC.

If any two of $Z_1, Z_3, Z_5$ in the numerator term in Equation (5) are capacitors with a capacitance value of $C$ and the rest are resistors $R$, Equation (5) becomes

$$Z_i = \frac{1}{s^2C^2R} \tag{6}$$

Thus, an FDNR with an element value of $D = C^2R$ can be realized.

Applying the Bruton Transformation to the prototype filter shown in **Figure 3** yields the circuit shown in **Figure 4**. Since this circuit behaves exactly the same as the prototype filter without the use of inductors, it can be easily integrated if the $D$ element, FDNR, is realized using active components.

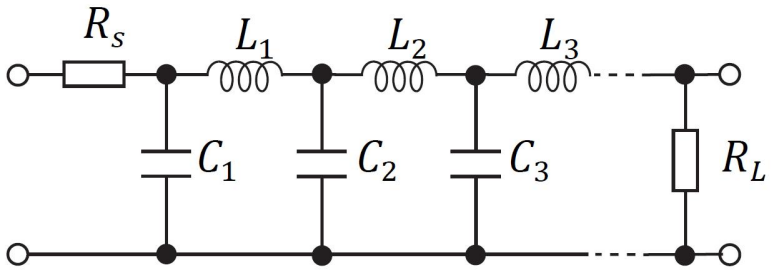


**Figure 3**. Prototype LPF.

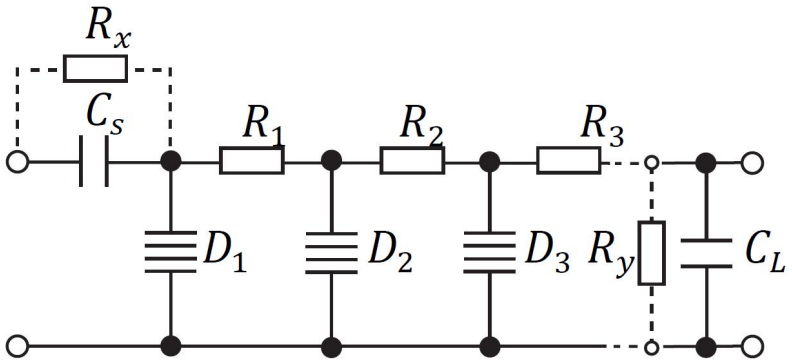


**Figure 4**. LPF with Bruton Transformation Applied.

Nevertheless, the circuit shown in **Figure 4** has one important problem. The terminal resistors $R_S$ and $R_L$ of the prototype filter are converted into capacitors $C_S$ and $C_L$ by Bruton Transformation. If the $D$ element in **Figure 4** is realized using the GIC shown in **Figure 2**, no DC bias is supplied to the operational amplifiers. This problem can be avoided by connecting $R_x$ in parallel to $C_S$, as shown by the dashed line in **Figure 4**. To reduce the passband gain error in the low frequency band, it is effective to connect $R_y$ in parallel to $C_L$ at the output termination [5]. In addition, to reduce the degradation of the filter characteristics over the entire frequency band, the resistances of $R_x$ and $R_y$ must be much larger than the impedance level of the filter components.

## 3. Various Configuration Methods for FDNRs

Since the first proposal of FDNR using GIC, other FDNR configuration methods have been proposed to date. This section introduces some of the main FDNR configuration methods.

### 3.1. FDNR Configuration with Operational Amplifiers

In addition to the proposal of the GIC shown in **Figure 2**, various configuration methods using operational amplifiers have been proposed [6–22]. The circuit proposed by Molo is shown in **Figure 5** [23]. This circuit can be called a GIC consisting of a single operational amplifier. If the passive elements of this circuit satisfy

$$2Z_1 = Z_4 = Z_6 = R \tag{7}$$

$$Z_2 = Z_3 = Z_5 = \frac{1}{sC} \tag{8}$$

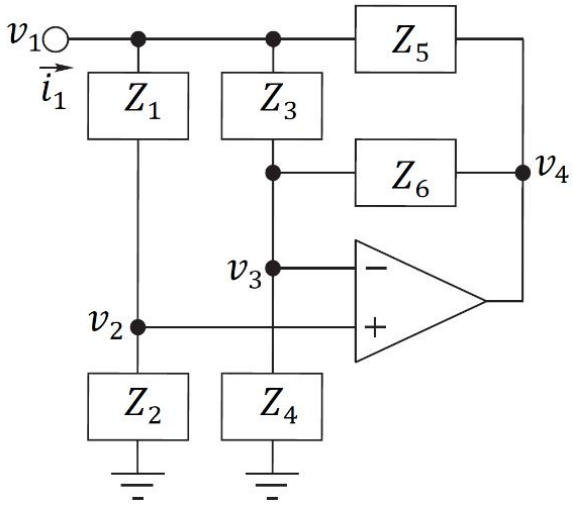


**Figure 5**. GIC with One Operational Amplifier.

The combined impedance is expressed as

$$Z_{in} = \frac{V_1}{i_1} = \frac{1}{s^2C^2R} \tag{9}$$

Compared to the GIC shown in **Figure 2**, this circuit can achieve FDNR with one operational amplifier, but it requires six passive elements, and more precise element value matching is required.

The circuit shown in **Figure 6** consists of fewer passive elements. The composite impedance is expressed as

$$Z_{\text{in}} = \frac{1}{s^2C_1C_2R + s(C_1 + C_2)} \tag{10}$$

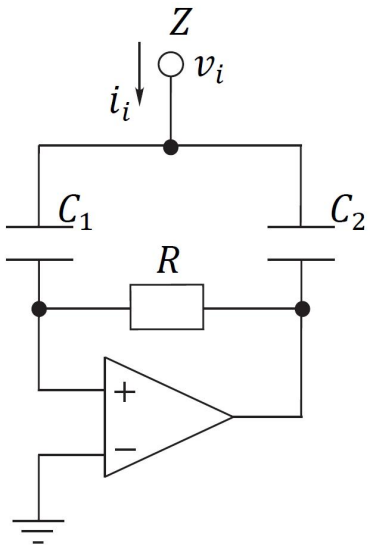


**Figure 6**. Lossy FDNR Circuit.

From this equation, it can be seen that the circuit shown in **Figure 6** can realize a composite element as shown in **Figure 7b**, in which a $D$ element with $D = C_1C_2R$ and a capacitor with capacitance $C = C_1 + C_2$ are connected in parallel [24]. This is the composite element obtained by applying Bruton Transformation to the parallel composite element of capacitor and resistor shown in **Figure 7a**. This parallel composite element can be regarded as a capacitor with loss, and thus the parallel composite element in **Figure 2b** is called a lossy FDNR. In contrast, a basic FDNR that realizes the impedance shown in Equations (6) and (9) can be called a lossless FDNR. The application of the lossy FDNR is limited to circuits that include a capacitor and a resistor in parallel connection inside the LC circuit. In order to achieve a lossless FDNR using a lossy FDNR, it is necessary to connect a negative impedance converter in parallel.

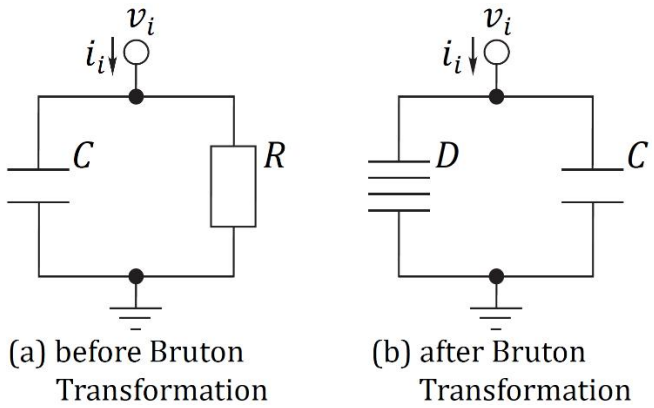


**Figure 7**. Lossy Composite Element; (**a**) Before Bruton Transformation and (**b**) After Bruton Transformation.

### 3.2. FDNR Configuration with Other Active Blocks

The circuit constructed using the Second-Generation Current Conveyors (CCIIs) shown in **Figure 8** functions as an FDNR, assuming the condition given by

$$C_2 = C_1\left(1 + \frac{R_3}{R_2}\right) \tag{11}$$

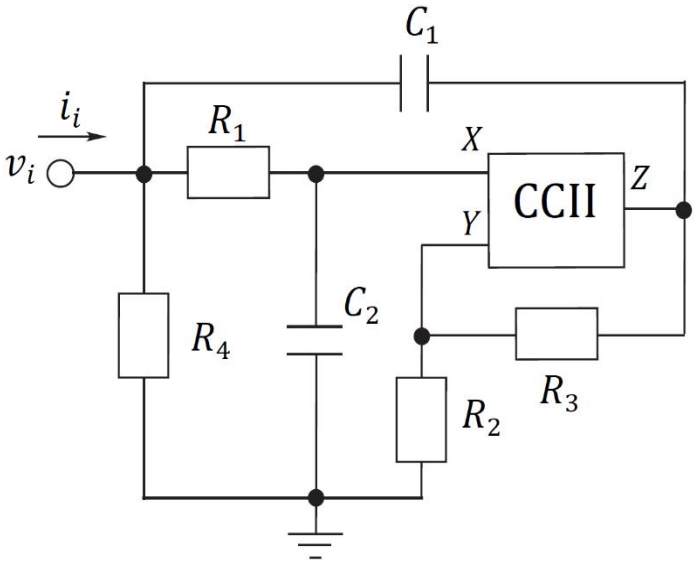


**Figure 8**. FDNR using CCII.

This circuit was proposed as a circuit to construct an oscillator [25]. If the relationship among the element values is set as

$$R_1 = R_3 = R_4 \tag{12}$$

$$R_2 = 2R_1 \tag{13}$$

The composite impedance is expressed as

$$Z_{\text{in}} = \frac{1}{s^2 3C_1^2 R_1} \tag{14}$$

and thus, this circuit functions as a lossless FDNR. On the other hand, if the relationship among the element values is set as

$$R_2 = R_1 = R_4 \tag{15}$$

The composite impedance is expressed as

$$Z_{\text{in}} = \frac{1}{s^2 C_1^2 R_1 \left(2 + \frac{R_1}{R_3}\right) + sC_1^2 R_1 \left(\frac{R_1 + R_3 + R_4}{R_4}\right)} \tag{16}$$

This equation means that this circuit functions as a lossy FDNR. Also after the proposition of this circuit, techniques for applying FDNR using CCII to oscillators have been proposed [26–28].

A method to realize a floating FDNR using CCII was proposed in 1983 [29]. The circuit configuration is shown in **Figure 9**. The impedance of this floating FDNR is expressed as

$$Z_D = \frac{v_1 - v_2}{i_1} = \frac{1}{s^2 C_1 C_2 R} \tag{17}$$

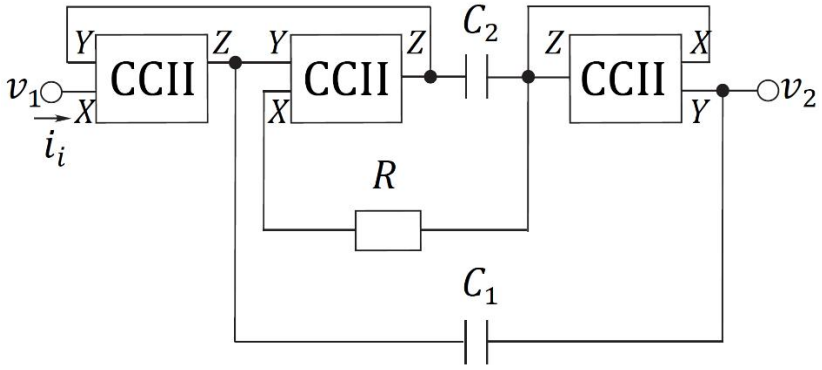


**Figure 9**. Floating FDNR using CCII.

It should be noted that while this circuit requires three CCII circuits, it uses only three passive elements. After this proposition, other techniques of constructing a floating FDNR using CCII have been proposed [30–34].

In the field of analog signal processing circuits in general, since the CCII circuit and its usefulness have been recognized, various derivative circuits based on CCII have been proposed. In this trend, various realization methods for FDNR using CCII-derived circuits, such as those using Second-Generation Current Controlled Current-Conveyor (CCCII) [35], Dual Output Second Generation Current Conveyors (DO-CCIIs) [36], Dual X Second-Generation Current Conveyors (DXCCIIs) [37], and Fully Differential Current Conveyor (FDCCII) [38], were proposed. The pioneer of the method was the realization technique using Second-Generation Current Controlled Current-Conveyor (CCCII) [35]. The circuit proposed by Abuelma'atti and Tasadduq is shown in **Figure 10** [35]. The CCCII is a CCII circuit with a series variable resistor built inside the X terminal. The resistance $R_{xi}(i = 1,2,3)$ in **Figure 10** is the variable resistance value of each CCCII, and is tuned by the control current $I_{bi}(i = 1,2,3)$. The composite impedance of this circuit is expressed as

$$Z_1 = R_{x1} + R_{x2} + \frac{1}{s^2 C_1 C_2 R_{x3}} \tag{18}$$

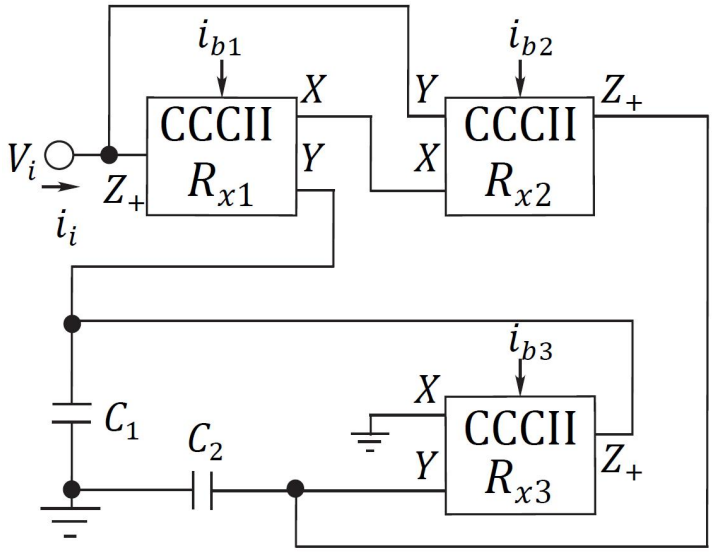


**Figure 10**. FDNR using CCCII.

In this equation, the third term represents the impedance of the lossless FDNR.

Various analog active blocks other than CCII-based blocks were also applied to realize FDNRs. The analog blocks utilized are as follows: Differential Voltage Current Conveyor (DVCC) [39,40], Differential Voltage Current Conveyer Transconductance Amplifiers (DVCCTA) [41], Current Backwards Trans-Conductance Amplifier (CBTA) [42], Voltage Differencing Transconductance Amplifiers (VDTA) [43–45], Voltage Differencing Current Conveyor (VDCC) [46–49], and Differential Voltage to Current Converter (DVTC) [50], Operational Floating Conveyors (OFC) [51], Differential-input Buffered and Transconductance Amplifier (DBTA) [52], Variable Gain Amplifier (VGA) [53], Current feedback operational amplifier (CFOA) [54–56].

While the configuration techniques introduced above can be summarized as combining active blocks with resistors and capacitors, methods that are not bound by that concept have also been proposed. Examples include the active- *R* method with operational amplifiers and resistors only [57], the method using multiple OTAs and capacitors [58], and the method using a new circuit called capacitive gyrator [59]. In addition to the method described in 3.1, the methods using operational amplifiers and DVCCs have also been proposed for FDNR oscillators [60–64]. Furthermore, FDNRs intended for application to switched capacitor filters have also been proposed [65–72].

## 4. Example of Integrated Filter Configuration Using Lossy FDNR

As described in 3.1, a lossy FDNR can be realized with a single operational amplifier, which is advantageous in terms of circuit size and power consumption compared to a lossless FDNR using a GIC that uses two operational amplifiers. In this section, examples of an integrated filter design using a lossy FDNR are presented.

### 4.1. Prototype Filter and Bruton Transformation

In the work by Tanimoto et al., a third-order resistive singly terminated lossy LC ladder filter is used as the prototype filter, as shown in **Figure 11** [73]. Applying the Bruton Transformation to the filter yields the result shown in **Figure 12**. The part surrounded by the dashed line can be realized with the lossy FDNR in **Figure 6**. Considering low element sensitivity, the prototype circuit should be a resistive doubly terminated filter. However, singly terminated filters also have an advantage, which is that there is no capacitor transformed from the input termination resistor $R_x$ in **Figure 4**. Thus there is no need for a high resistor for bias supply. In addition, the filter proposed by

Tanimoto et al. has one more advantage that the filter does not generate an offset voltage in principle [73]. If the part surrounded by the dashed line in **Figure 12** is realized with the FDNR in **Figure 6**, the offset of the operational amplifier does not affect the output of the filter because the capacitor breaks up the DC path. Nevertheless, the operating bias of the operational amplifier is self-contained. This is an important property for its introduction into portable communication devices.

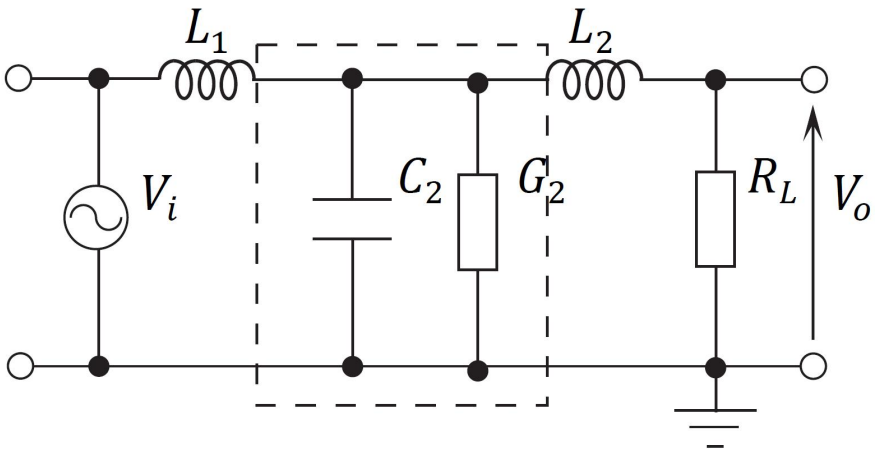


**Figure 11**. 3rd Order LPF.

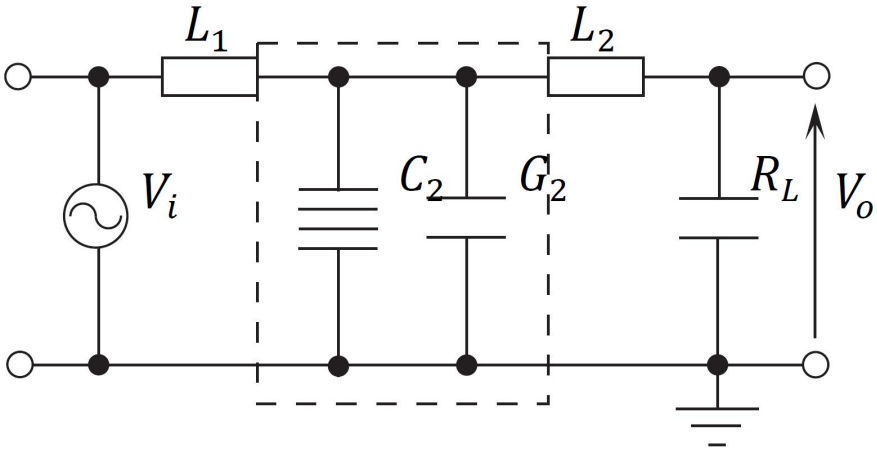


**Figure 12**. 3rd Order LPF After Bruton Transformation.

### 4.2. Filter Using Lossy FDNR with CCII

**Figure 13** illustrates the lossy FDNR proposed by the authors' group [74]. A CCII and a Multi-Output CCII (MOCCII) are employed as active blocks. The lossy FDNR is applied to a third-order low-pass filter as shown in **Figure 14**. The prototype circuit is the filter shown in 11. The parts surrounded by dashed lines in both figures correspond each other.

The voltage and the current characteristics of MOCCII and CCII are respectively given as

$$\begin{bmatrix} V_x \\ I_y \\ I_{z1} \\ I_{z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha & 0 & 0 & 0 \\ \beta & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_{z1} \\ V_{z2} \end{bmatrix} \tag{19}$$

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ \gamma & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \end{bmatrix} \tag{20}$$

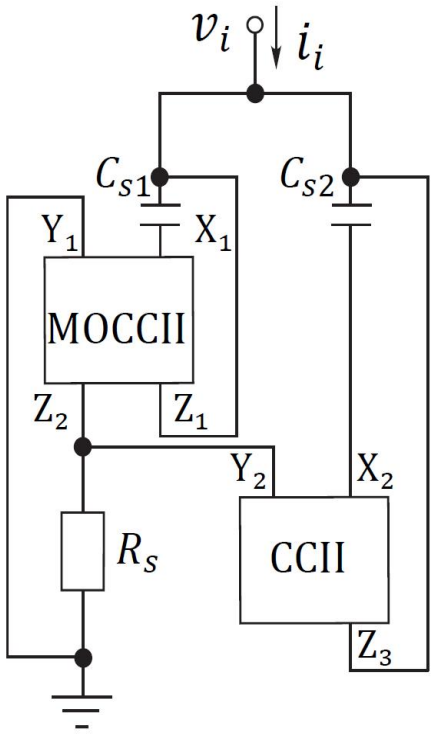


**Figure 13**. Lossy FDNR Proposed by Matsumoto [74].

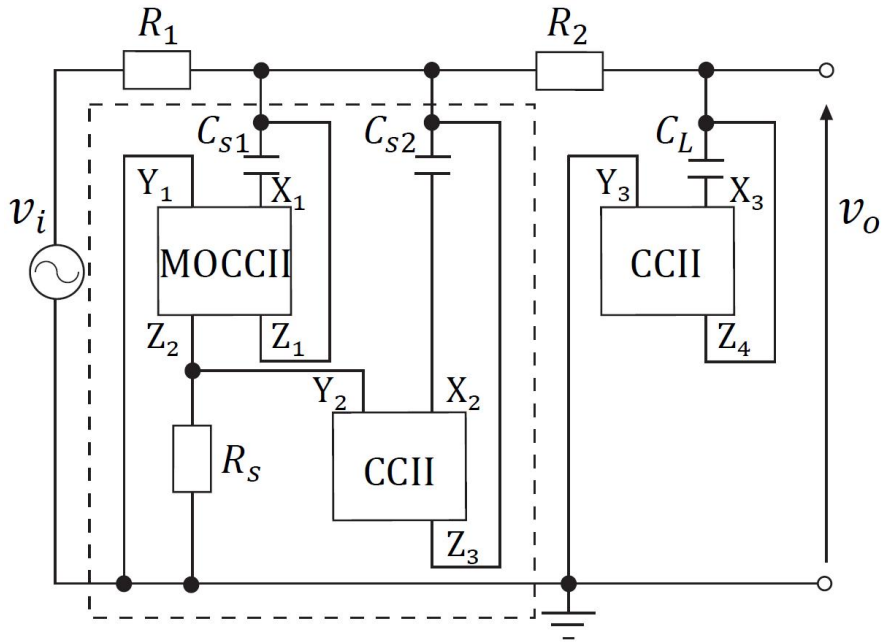


**Figure 14**. 3rd Order LPF with Lossy FDNR.

Although the gain of the current transfer characteristic of CCII is 1 generally, in this filter, the gains are set to $\alpha$ and $\beta$ for the MOCCII, and $\gamma$ for the CCIIs. The purpose is to provide the function of a capacitance multiplier, by which the large capacitance required for a low frequency filter is realized even with a small capacitor [75].

The CCII with $C_L$ in **Figure 14** is the capacitance multiplier that increases the capacitance $C_L$ by a certain factor. The diagram of that part is shown again in **Figure 15**. With the current amplification factor from the X terminal to the Z terminal as $\gamma$, the combined impedance of this circuit is expressed as

$$\frac{v_i}{i_i} = \frac{v_i}{i_x + i_z} = \frac{v_i}{sC_L v_i + \gamma sC_L v_i} = \frac{1}{\mathrm{s}(1+\gamma)\mathrm{C_L}} \tag{21}$$

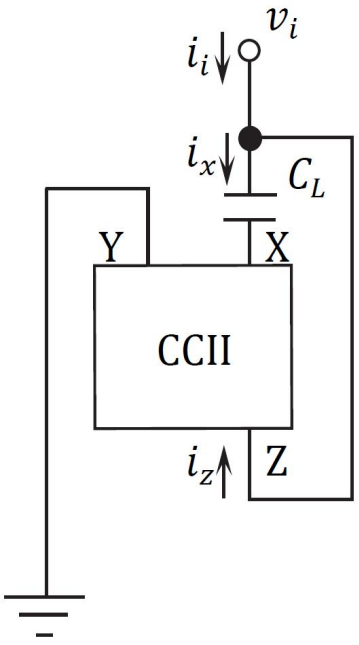


**Figure 15**. How to Scaling.

In this way, the capacitance multiplier is a circuit that lowers the substantial impedance by the amplified signal current to achieve $(1+\gamma)$ times the capacitance. The CCII and the MOCCII the lossy FDNR also operate based on the same principle to make the connected capacitance $C_{s1}$ and $C_{s2}$ appear larger. The function of the Z 2 terminal of MOCCII is similar to the capacitance multiplier in basic principle, and in this FDNR, the resistance $R_S$ can be reduced by a factor of $1/\beta$ due to the current amplification factor $\beta$.

Considering the current amplification factors $\alpha, \beta$, and $\gamma$, the composite impedance of the lossy FDNR shown in **Figure 13** is expressed as

$$T(s) = \frac{1}{\begin{matrix} s^2(1+\alpha)C_{s1}(1+\gamma)C_{s2}\beta R_s \\ +s[(1+\alpha)C_{s1} + (1+\gamma)C_{s2}] \end{matrix}} \tag{22}$$

By setting the coefficients to large values, the capacitances and the resistance can be reduced to small values without changing the composite impedance.

### 4.3. Element Value of Filter

Although the calculation method for deriving the element values of the LC ladder filters is complicated, it has already been established [76]. However, the method assumes that the elements other than the terminating resistors are reactance elements. Thus, no systematic design method has been found for LC filters in which loss is added to the reactance element, as shown in **Figure 11**. For relatively low order filters (empirically 4th order or lower), it is

possible to obtain the element value by comparing the coefficients of the denominator polynomial of the desired transfer function and the transfer function derived from the prototype filter with the loss [77].

As a design example, consider the third-order Butterworth characteristic realized by the prototype filter shown in **Figure 11**. The transfer function of the third-order Butterworth characteristic is as follows:

$$T(s) = \frac{1}{s^3 + 2s^2 + 2s + 1} \tag{23}$$

On the other hand, the transfer function of the prototype filter is as follows:

$$T(s) = \frac{1}{A_3 s^3 + A_2 s^2 + A_1 s + 1} \tag{24}$$

$$A_1 = L_1 L_3 C_2 \tag{25}$$

$$A_2 = L_1 (G_2 L_3 + C_2) \tag{26}$$

$$A_3 = L_1 G_2 + L_1 + L_3 \tag{27}$$

where the value of the termination resistor $R_L$ is set to 1, and $G_2 = 1/R_2$. Comparing the filter in **Figure 11** with a lossless LC filter, an extra loss resistance $R_2$ of the capacitor $C_2$ is added, thus the number of element value variables increases by one. This means that there is one degree of freedom in design. Here, using the loss factor $\delta$, the variable is transformed as

$$\frac{1}{R_2} = \delta C_2 \tag{28}$$

By comparing the coefficients of Equations (23) and (24), simultaneous equations are obtained. Solving the equations for each element value, the following solutions are obtained:

$$L_1 = \frac{3 - 6\delta + 4\delta^2 - \delta^3}{2 - \delta} \tag{29}$$

$$L_3 = \frac{1}{2 - \delta} \tag{30}$$

$$G_2 = \delta C_2 = \frac{\delta (2 - \delta)^2}{3 - 6\delta + 4\delta^2 - \delta^3} \tag{31}$$

Once the value of $\delta$ is determined, the element value can be derived from (31). Here, the condition for determining the value of $\delta$ is set as $L_1 = L_3$. From Equations (29) and (30), the solution is $\delta = 0.456311$. This results in element values of $L_1 = L_3 = 0.6478$ and $G_2 = 1.0874$.

The composite impedance of the part surrounded by the broken line in **Figure 12** is expressed as

$$\frac{v_i}{i_i} = \frac{1}{s^2 C_2 + s G_2} \tag{32}$$

On the other hand, that in **Figure 9** is expressed as

$$\frac{v_i}{i_i} = \frac{1}{s^2 C_{s1} C_{s2} R_s + s(C_{s1} + C_{s2})} \tag{33}$$

where it is here assumed that the capacitance multiplier and the resistance reduction function do not operate, namely, $\alpha = \gamma = 0$ and $\beta = 1$. These multiplication factors are applied after frequency scaling and impedance scaling of the normalized element values taking into account the possibility of implementing on an IC chip.

Comparing the coefficients in Equations (32) and (33), the following simultaneous equations are obtained:

$$\begin{cases} C_2 = C_{s1}C_{s2}R_s \\ G_2 = C_{s1} + C_{s2} \end{cases} \tag{34}$$

In the lossy FDNR shown in **Figure 13**, the number of passive elements is three, thus the degree of freedom in design increases by one more. Here, setting $C_{s1} = C_{s2}$ and solving Equation (34) yields $C_{s1} = C_{s2} = 0.5437$ and $R_S = 8.0615$.

The cutoff frequency of the filter is set to 1 kHz for use as an anti-aliasing filter for electromyographs. Setting resistances $R_1$ and $R_3$ to 200 kΩ, the following values are obtained by scaling the element values described above:

$$\begin{cases} R_1 = R_3 = 200\ \text{k}\Omega \\ R_s = 24.9\ \text{M}\Omega \\ C_{s1} = C_{s2} = 281\ \text{pF} \\ C_L = 515\ \text{pF} \end{cases} \tag{35}$$

As shown in this element value list, the values of the capacitances and resistor $R_s$ are too large to be implemented on an IC chip. Therefore, further scaling is performed by the capacitance multiplier and the resistance reduction function using the current amplification factor, $\alpha, \beta$ and $\gamma$ of CCII and MOCCII. By setting $\alpha = \gamma = 9$, the apparent capacitance value can be increased by a factor of 10 from Equation (21), thus the capacitance of each capacitor can be reduced to 1/10. Similarly by setting $\beta = 10$ without changing the signal voltage at the $Z_2$ terminal of MOCCII, the value of $R_S$ can be reduced to 1/10. Each element value obtained in this way is shown again below:

$$\begin{gathered} R_1 = R_3 = 200\ \text{k}\Omega \\ R_s = 2.49\ \text{M}\Omega \\ C_{s1} = C_{s2} = 28.1\ \text{pF} \\ C_L = 51.5\ \text{pF} \end{gathered} \tag{36}$$

These reduced element values contribute to reducing the area of passive elements implemented on the chip.

Detailed circuit diagrams of CCII and MOCCII used in this filter are shown in **Figures 16** and **17**, respectively. The values of current amplification factors $\alpha, \beta$ and $\gamma$ for CCII and MOCCII are set by the gate widths of transistors M9-12 in CCII and M9-12 and M13-16 in MOCCII, respectively.

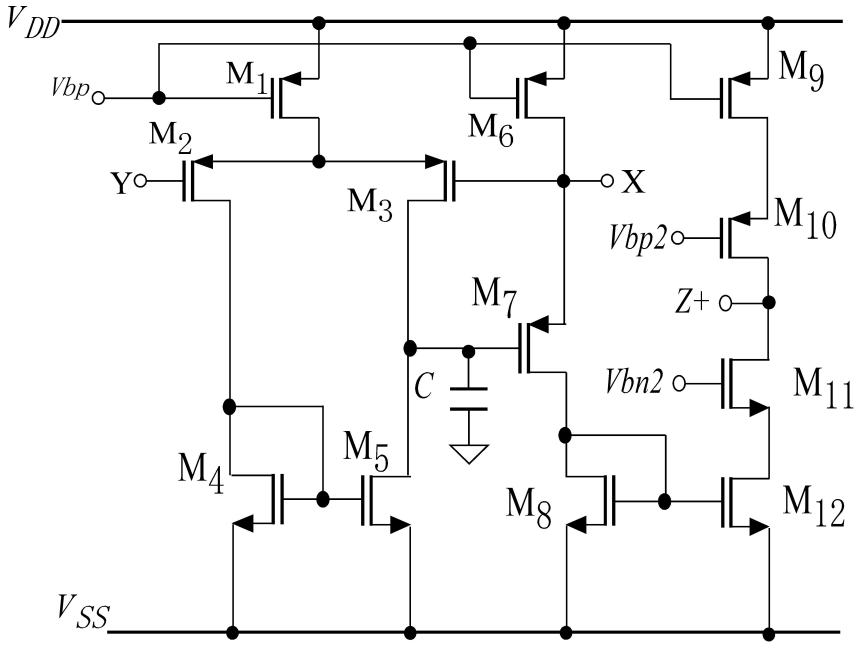


**Figure 16**. Circuit Diagram of the CCII+.

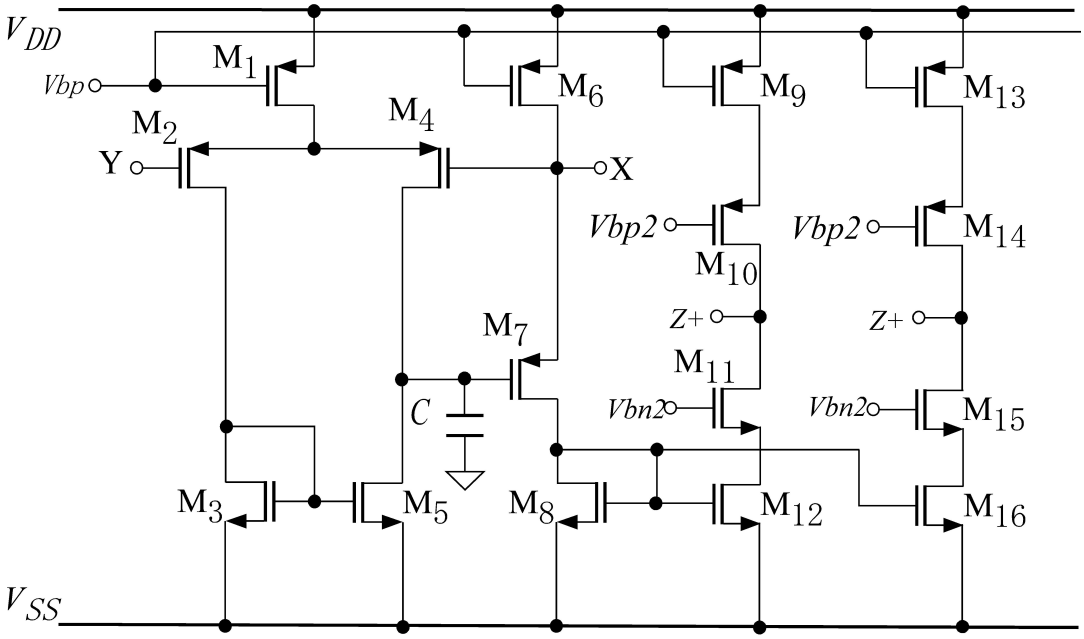


**Figure 17**. Circuit Diagram of the MOCCII+.

## 4.4. Characteristics

Simulations were performed using the circuit simulator LTspice. The filter is undergoing integration in a 0.6$\mu$ m process using a chip prototyping service for universities. The 0.6$\mu$ m process BSIM3v3 was used as the transistor model for the simulation.

To construct a circuit with the same function as the lossy FDNR shown in **Figure 13** through conventional method, floating capacitance multipliers would be applied to the two capacitors in the circuit of **Figure 6**. Several methods of constructing floating capacitance multipliers are known, and recently the authors' group has proposed the circuit configuration shown in **Figure 18** [78]. The operational amplifier used in the conventional circuit is the circuit shown in the work by Tanimoto et al. [73].

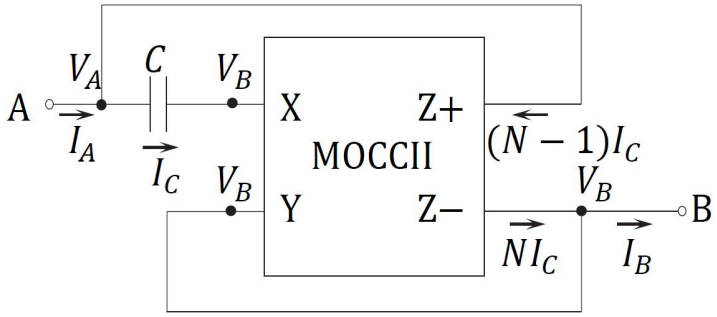


**Figure 18**. Floating Capacitance Multiplier Constructed of an MOCCII.

**Figure 19** shows the gain characteristics. The solid red line, the dotted blue line and the dashed green line represent the characteristics of the proposed circuit, the conventional circuit, and the theoretical value, respectively. This figure shows that the third-order Butterworth slow-pass characteristic has been achieved. **Figure 20** shows the temperature characteristic. The first order and the second order temperature coefficients of resistance are TC1 = 1000 ppm/ ˚C and TC2 = 10ppm/ ˚C, respectively.

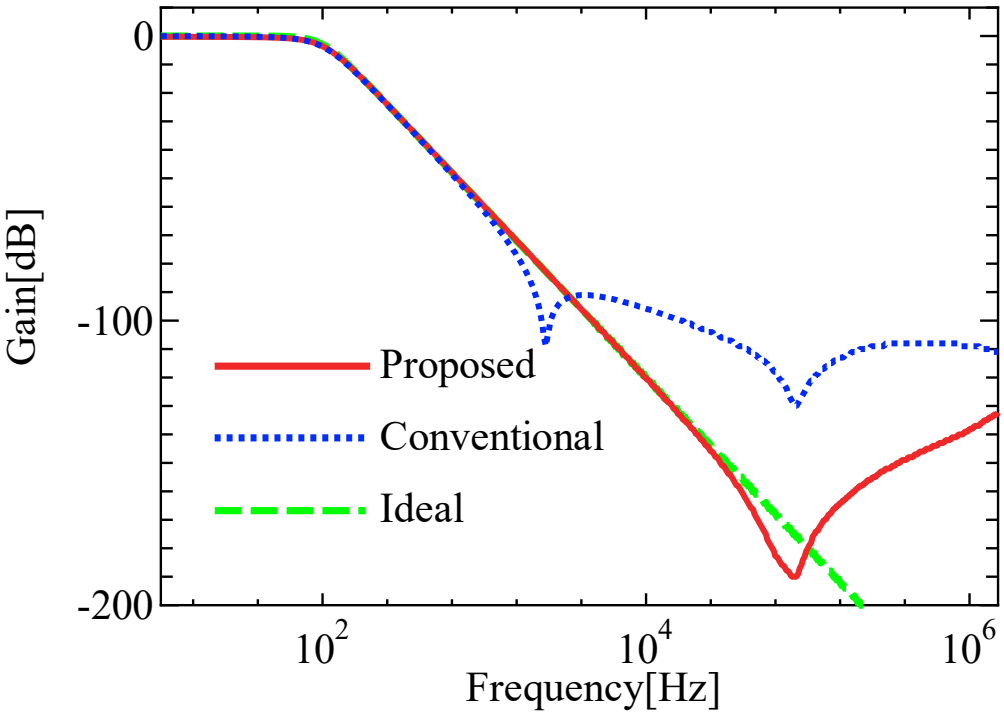


**Figure 19**. Amplitude Characteristics.

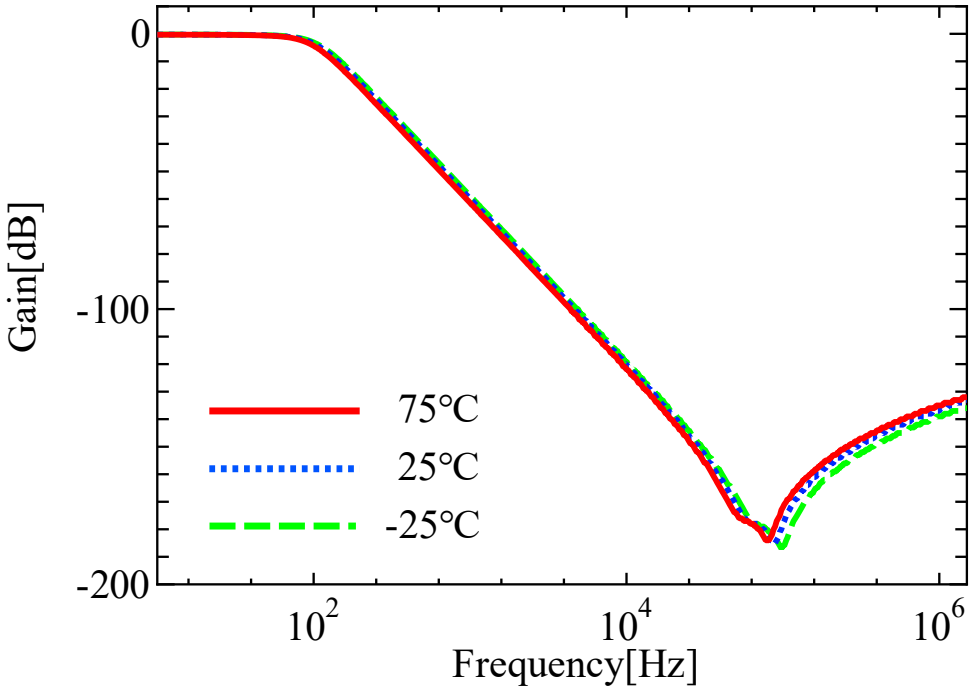


**Figure 20**. Temperature Characteristic of Proposed Filter.

The result of the transient analysis of the proposed circuit is illustrated in **Figure 21**. The frequency of the input signal is 100 Hz. The dashed blue line indicates the input voltage and the solid red line indicates the output voltage. This figure shows that the filter circuit operates stably without oscillation and that the amplitude of the signal with the frequency equal to the cutoff frequency is −3 dB. **Table 1** summarizes other results, where $V_{\max}$ is the maximum input voltage at which the THD of the output signal is less than 5%, and $V_{\text{noise}}$ is the input referred noise between 1 Hz and 1 MHz. These results show that the proposed circuit is superior to the circuit constructed by the conventional method.

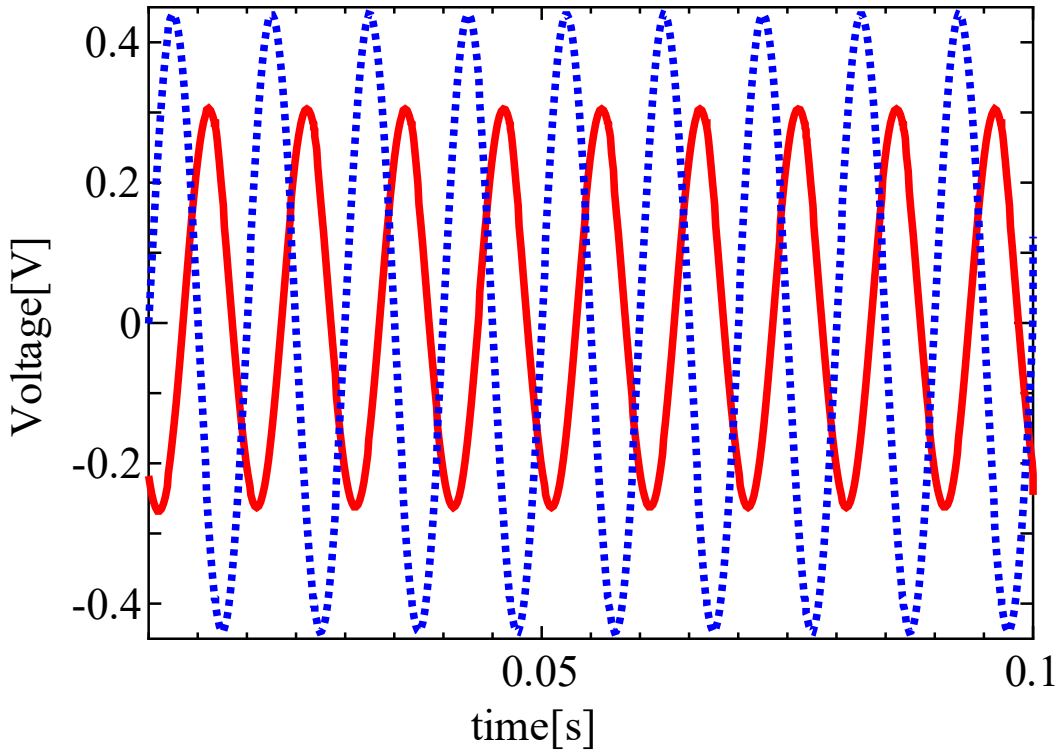


**Figure 21**. Input and Output Signals of Proposed Filter.

**Table 1**. Other Results of Filters.

| | **Proposed** | **Conventional** |
|---|---|---|
| Power | 146 $\mu$ W | 177 $\mu$ W |
| $V_{\max}$ | 0.44 V | 0.24 V |
| $V_{\text{noise}}$ | 3.3 mV | 4.4 mV |
| S/N | 42 dB | 37 dB |

## 5. Conclusion

This paper has provided an overview of the Bruton Transformation and FDNRs, and introduces recent design example. The FDNR is a special element generated by the Bruton Transformation. Its impedance is a negative impedance that depends on $\omega^2$. Since such an element does not exist as a passive element, it is realized by using active blocks.

The first half of this paper has presented examples of various FDNR configurations that had been proposed since FDNR first appeared with the Bruton Transformation. With the help of the active block function, various efforts have been made to generate a function equivalent to the square of the impedance of the capacitor. Most of them consist of adding passive elements to existing active blocks such as operational amplifiers and CCIIs. However, it is also emerging that attempts to constitute an FDNR with a small number of passive elements and active blocks are concentrated in a limited number of configuration methods. The trend in research has shifted to a variety of active blocks derived from the well-known active blocks, operational amplifiers and CCIIs, with the aim of improving FDNR characteristics and adding functions such as tunability. Incidentally, the first proposed GIC is still in use today because it exhibits very good characteristics within the operating bandwidth of the operational amplifier employed.

On the other hand, a new circuit called lossy FDNR has appeared. The authors imagine that this may be the result of leaving the loss component uncanceled in the research process of lossless FDNR and developing a new use for it. Lossy FDNRs have a great advantage over lossless FDNRs in that they can generally be configured with fewer active blocks. The second half of this paper has presented an example of a method for integrating LC filters using its lossy FDNR. The filter is composed of CCIIs including an MOCCII as active blocks. For low frequency applications, the CCIIs have current amplification factors to realize capacitance multiplier function that increases the apparent capacitance from a capacitor with a small capacitance, thereby reducing the area of elements implemented on IC chip.

Although the Bruton Transformation seems to be a minor method of integrating LC filters compared to gyrator-C type and leapfrog filters, there is a good possibility that circuit configurations and design methods will emerge that take advantage of its strengths. The author's group is studying several other lossy and lossless FDNRs and will publish them in due course in the near future.

## Author Contributions

Conceptualization, F.M.; data curation, F.M. writing-original draft preparation, F.M. and T.I.; writing-review and editing, F.M.; analysis and classification of conventional methods, T.I., organizing references, T.I. All authors have read and agreed to the published version of the manuscript.

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## Data Availability Statement

All data are shown in the authors' published papers cited in this paper.

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## Conflicts of Interest

The authors declare no conflict of interest.

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